DEVELOPMENT AND APPLICATION OF AN EMPIRICAL THYRISTOR TYPE SWITCH MODEL FOR PULSE GENERATOR SIMULATION

by

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CONTENTS

ABSTRACT

Recent developments in semiconductor design and fabrication have led to the realization of more robust thyristor-type silicon switches. A single device is capable of holding off up to 4 kV and switching up to 14 kA for single pulses, or 10 kA for repetitive pulses. These switches may be used to design pulse generators that do not utilize any traditional gaseous high power switches, leading to more compact generators with longer lifetimes, greater reliability, less jitter, and that require less maintenance.

Simulation of a pulse generator is often useful for design evaluation and optimization before construction. However, the validity of simulation results is dependent on the accuracy of the models used to describe the nonlinear components in the circuit. To this end, an empirical SPICE model is developed for Silicon Power's CCS SC 14N40 thyristor-type switch. The development of the model is detailed, and SPICE simulations of the model are compared to experimental measurements with reasonable agreement. The model is intended for use in evaluation of the performance of a linear transformer driver (LTD) type pulse generator as a possible driver for a virtual cathode oscillator (vircator) high power microwave generator.

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

The development of semiconductor technology has allowed for the design and production of a wide range of compact, robust, and reliable devices that have replaced many traditional components. Until recently, most high power pulse generators utilized gaseous discharges to switch high currents and voltages. The maturation of power semiconductor technology has enabled the fabrication of robust solid-state switches that can replace traditional gaseous discharge switches in many pulse generator designs. Thyristor-type switches in particular stand out as the most robust switches for pulsed power applications. Silicon Power Inc. has designed and fabricated thyristor switches capable of up to 4 kV voltage hold-off and up to 14 kA pulsed current conduction [1].

As computational capabilities have grown, several powerful circuit simulation programs have been developed, such as the SPICE simulators. Designers often use such simulation softwares to evaluate a design's performance before spending resources and time on construction. To analyze circuits containing nonlinear components, such as semiconductor devices, a given device's behavior may be described in a SPICE subcircuit, which appropriately models the characteristics of the device.

Models currently exist for thyristor type switches [2, 3, 4, 5]. Some models are convenient to implement in a SPICE simulator, but are overly simplistic and do not accurately characterize the transient turn-on performance of the switch [2]. Other

models may be highly accurate and based on first principles, but are difficult and impractical to implement in a SPICE simulation, and may require proprietary information about the switch such as doping profiles and device geometry [3, 4]. One empirical model in particular demonstrates accurate performance and ease of implementation, but the model is only valid for a single set of circuit parameters (such as load and discharge capacitance) [5].

A high power pulse generator is necessary for the development of a virtual cathode oscillator (vircator) high power microwave generator [6]. Currently, a Marx generator has been developed to provide the driving pulse, but a linear transformer driver (LTD) may serve as a superior, more compact pulse generator. As power semiconductor technology has matured, solid-state LTDs have been developed that demonstrate the utility of such devices [7, 8]. Before a solid-state, thyristor switched LTD is designed and constructed, it is desirable to approximate the generator's performance. To this end, a SPICE model for Silicon Power's CCS-SC-14N40 thyristor-type switch is developed to accurately characterize the transient off-to-on performance of the switch in such a generator.

CHAPTER 2

THEORETICAL BACKGROUND

In order to accurately model a semiconductor device, the physical operation of the device must be considered. Basic semiconductor principles, an understanding of thyristor operation, and knowledge of previous thyristor models and their strengths and shortcomings lend insight into how the device can be modeled.

2.1 Semiconductor Basics

Semiconductors are a special class of materials characterized by resistivity less than insulators and greater than metals. Semiconductors generally possess a smaller energy gap between the valence band, where electrons are bound to their host atoms, and the conduction band, where electrons are free to flow. Table 2.1 lists the band gap in electron volts (eV) for common semiconductors at 300 K [9].

These materials possess band gap energies much lower than the ionization energies of gasses, which may be in the tens of electron volts [10], but simultaneously possess relatively few free charge carriers (1.5×10^{10} cm^{-3} for Si at 300 K), unlike metals, which have much higher charge carrier densities (8.5×10^{22} cm^{-3} for Cu). Furthermore, their molecular structure enables manipulation of electrical properties via manipulation of the chemical composition.

Table 2.1: Bandgap energy for various semiconductors at 300 K.

Semiconductor	Bandgap Energy
Si	1.11 eV
Ge	0.66 eV
InSb	0.17 eV
InAs	0.36 eV
InP	1.27 eV
GaP	2.25 eV
GaAs	1.43 eV
GaSb	0.68 eV
CdSe	1.74 eV
CdTe	1.44 eV
ZnO	3.2 eV
ZnS	3.6 eV

2.1.1 Intrinsic Semiconductors

On the microscopic level, semiconductors are a lattice of covalently bonded atoms. Semiconductors used for electronics are grown as a single crystal, with very few free charge carriers available for conducting electric current. The free charge carrier density of an intrinsic semiconductor at a given absolute temperature is given by Eq. 2.1 [11].

$$n_i^2 = BT^3 e^{-E_G/(k_B T)} \tag{2.1}$$

Here, n_i is the intrinsic semiconductor free charge carrier density (cm^{-3}), T is the absolute temperature (K), E_G is the band gap energy (eV), k_B is the Boltzmann constant (8.62×10^{-5} eV/K), and B is a material-dependent parameter (5.4×10^{31} K^{-3} for silicon). At room temperature (300 K), the free charge carrier density of silicon is 1.5×10^{10} cm^{-3}.

Two types of free charge carriers exist in semiconductors. First, free electrons are electrons that are not part of a covalent bond, and thus exist in the conduction band. Second, holes are locations in the lattice where an electron is missing, resulting in a net positive charge. Free electrons and holes are depicted in a simplified diagram in Fig. 2.1. Free electrons and holes travel by means of two mechanisms known as drift and diffusion.

Diffusion is a macroscopically observable change in the volumetric particle density that occurs as a result of the random microscopic movement of particles. Diffusion only occurs when the gradient of the density is nonzero ($\nabla n(\vec{\boldsymbol{r}}) \neq 0$). Diffusion is characterized by Eq. 2.2.

$$\frac{\delta n(\vec{\boldsymbol{r}}, t)}{\delta t} = \nabla \cdot [D \nabla n(\vec{\boldsymbol{r}}, t)] \tag{2.2}$$

Here, n is the density of the particles in question (m^{-3}), which varies with location $\vec{\boldsymbol{r}}$ (m) and time t (s). D is the diffusion coefficient (m^2/s), which is given in terms of

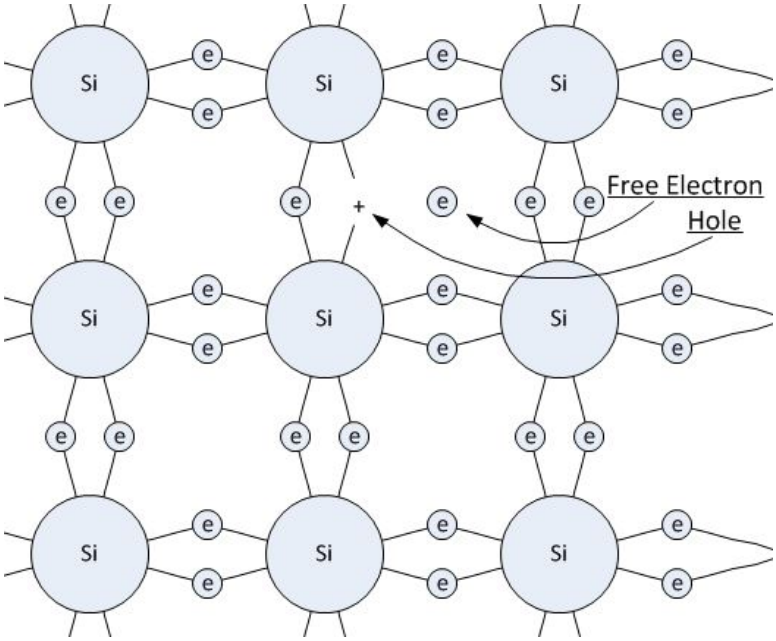

Figure 2.1: Simplified illustration of charge carriers in intrinsic silicon.

the charge carrier mobility μ (m^2/Vs) and the thermal voltage (V) according to Eq. 2.3.

$$D = \mu V_T = \frac{\mu k T}{q_e} \tag{2.3}$$

The charge carrier mobility μ, and thus the diffusion constant D, are specific to the type of charge carrier, and indicated by a subscript p for holes or n for electrons.

The diffusion of charge carriers results in an electric current known as the diffusion current. Since diffusion is a volumetric process, it is convenient to refer to diffusion current as a volumetric current density $\vec{\boldsymbol{J}}_{p,diffusion}$ or $\vec{\boldsymbol{J}}_{n,diffusion}$ (A/m^2). Eq. 2.4 gives the relation between the diffusion coefficient and volumetric charge carrier distribution.

$$\vec{\boldsymbol{J}}_{p,diffusion} = -q_e D_p \nabla n_p(\vec{\boldsymbol{r}}, t)$$

$$\vec{\boldsymbol{J}}_{n,diffusion} = q_e D_n \nabla n_n(\vec{\boldsymbol{r}}, t) \tag{2.4}$$

It is noted that in reality the diffusion of charge carriers becomes more complicated than the relation given in Eq. 2.2. Because electron mobility in intrinsic silicon is roughly three times that of hole mobility ($\mu_p = 480$ cm^2/Vs and $\mu_n = 1350$ cm^2/Vs at 300 K), a local concentration of electrons and holes will experience a net negative current away from the region as electrons diffuse away from the region more quickly than holes. This results in the development of a positive space charge in the region, generating an electric field pointing away from the region. This electric field acts upon the electrons, impeding their further diffusion, and the holes, accelerating their diffusion. This phenomenon is known an as ambipolar diffusion, and is beyond the scope of this thesis.

Drift refers to the movement of charge carriers due to the presence of an electric field $\vec{\boldsymbol{E}}$ (V/m). The drift speed $|\vec{\boldsymbol{v}}|$ (m/s) of a charged particle is directly proportional to the electric field strength $|\vec{\boldsymbol{E}}|$ (V/m), as given in Eq. 2.5.

$$\vec{\boldsymbol{v_p}} = \mu_p \vec{\boldsymbol{E}}$$

$$\vec{\boldsymbol{v_n}} = -\mu_n \vec{\boldsymbol{E}} \tag{2.5}$$

The drifting process occurs differently for electrons and holes. A drifting electron travels in the direction opposite of the electric field, and is impeded by lossy inter-

actions with nearby atoms in the crystal lattice. Holes drift via the movement of electrons: an electron adjacent to the hole experiences a coulomb force due to the presence of the positive hole, and moves over to fill the hole, resulting in a new hole where the electron was previously located. This occurs in a sequential manner as the hole moves. The current density that results from free charge carriers in an electric field is given in 2.6.

$$\begin{aligned} \vec{\boldsymbol{J}}_{p,drift} &= q_e n_p(\vec{\boldsymbol{r}}, t)\mu_p \vec{\boldsymbol{E}} \\ \vec{\boldsymbol{J}}_{n,drift} &= q_e n_n(\vec{\boldsymbol{r}}, t)\mu_n \vec{\boldsymbol{E}} \end{aligned} \tag{2.6}$$

It is noted that Eq. 2.6 can be rearranged to given an expression for the bulk resistivity of an intrinsic semiconductor. By definition, the bulk resistivity of an isotropic material is the ratio of $|\vec{\boldsymbol{E}}|/|\vec{\boldsymbol{J}}|$. Eq. 2.6 can be combined and rearranged to give the bulk resistivity of an intrinsic semiconductor, given in Eq. 2.7. For intrinsic silicon at 300 K, the bulk resistivity is roughly $2.27\,\mathrm{k\Omega\,m}$.

$$\rho(\vec{\boldsymbol{r}}, t) = \frac{|\vec{\boldsymbol{E}}|}{|\vec{\boldsymbol{J}}|} = \frac{1}{q_e(\mu_p n_p(\vec{\boldsymbol{r}}, t) + \mu_n n_n(\vec{\boldsymbol{r}}, t))} \tag{2.7}$$

The total current density in the semiconductor is then a superposition of electron diffusion, hole diffusion, electron drift, and hole drift, as shown in Eq. 2.8.

$$\begin{aligned}\vec{\boldsymbol{J}}_{total} = &- q_e D_p \nabla n_p(\vec{\boldsymbol{r}}, t) + q_e D_n \nabla n_n(\vec{\boldsymbol{r}}, t) \\ &+ q_e n_p(\vec{\boldsymbol{r}}, t)\mu_p \vec{\boldsymbol{E}} + q_e n_n(\vec{\boldsymbol{r}}, t)\mu_n \vec{\boldsymbol{E}} \end{aligned} \tag{2.8}$$

2.1.2 Doped Semiconductors

Intrinsic semiconductors alone do not provide the electrical characteristics necessary to build modern semiconductor devices. To alter the electrical properties of intrinsic semiconductors, impurities are introduced into the crystal lattice. Silicon, for example, forms a tetrahedral crystal lattice in which each atom is bound to four neighboring atoms. Since silicon atoms possess four valence electrons, this results in no free charge carriers, besides those that exist due to thermal population (see Eq. 2.1).

If an atom possessing five valence electrons (such as phosphorus) replaces a silicon atom, it will covalently bond with the four available neighbors, but one electron will be unbound, and is available to carry charge. Semiconductors that are doped with impurities that increase the free electron density are said to be n-type semiconductors, because negatively charged electrons are the majority free charge carrier. A simplified diagram of charge carriers in n-type silicon is shown in Fig. 2.2.

Alternatively, if an atom possessing three valence electrons (such as boron) replaces a silicon atom, it will covalently bond with only three of the available four neighboring atoms. This creates a hole, where a free electron may attach to the boron atom and complete a fourth covalent bond with a neighboring atom. Semicon-

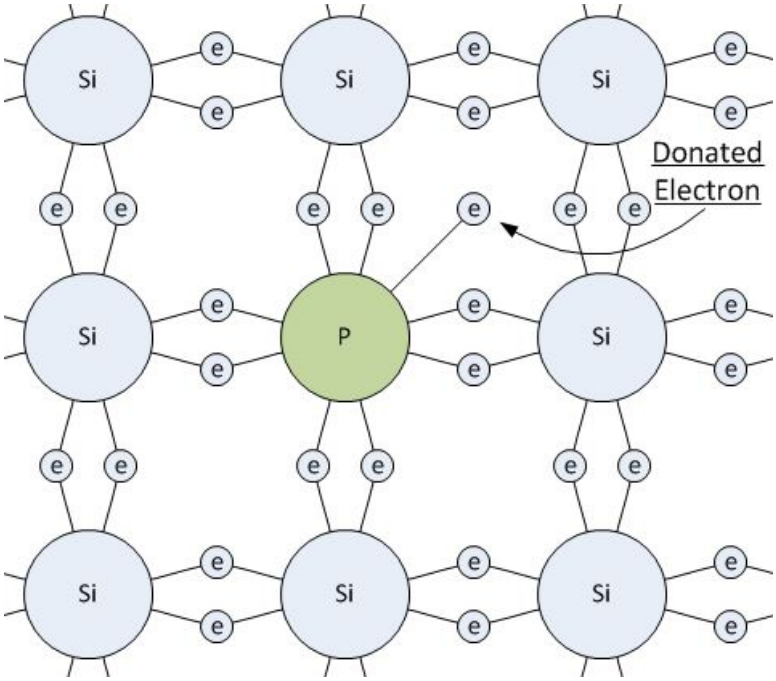

Figure 2.2: Simplified illustration of charge carriers in n-type silicon.

ductors that are doped with impurities that increase the hole density are said to be p-type semiconductors, because positively charged holes are the majority free charge carrier. A simplified diagram of charge carriers in p-type silicon is shown in Fig. 2.3.

It is noted that doped semiconductors are electrically neutral. A surplus of free charge carriers of a particular polarity does not indicate a lack of charge of the opposite polarity, only that the opposite polarity charge is not free to flow. In the case of n-type semiconductors, for every donated free electron, a proton is bound in the nucleus of the donor atom. In the case of p-type semiconductors, for every hole there is one less proton in the nucleus of the acceptor atom.

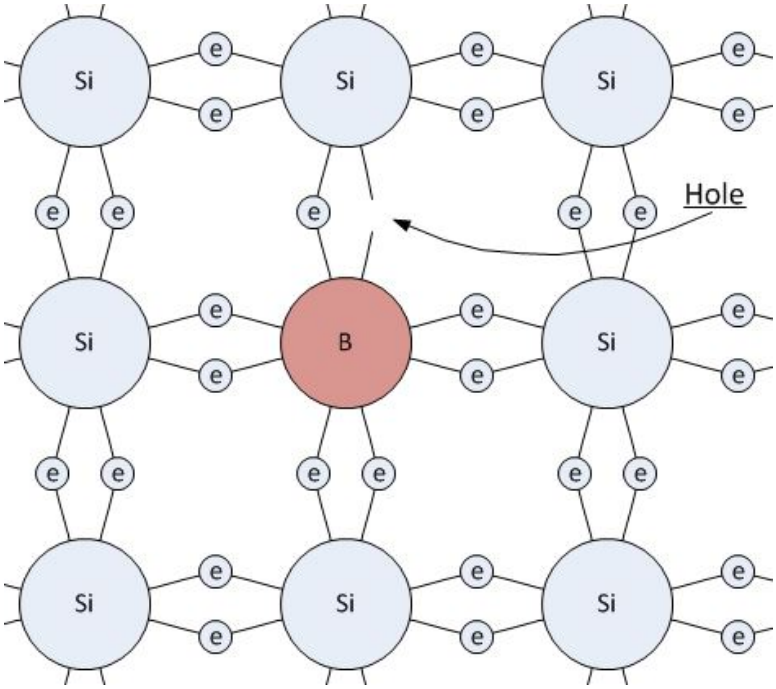

Figure 2.3: Simplified illustration of charge carriers in p-type silicon.

2.1.3 pn Junctions

The properties of doped semiconductors are of particular interest where an n-type region shares a boundary with a p-type region. The end of one type and the beginning of the opposite type necessarily creates a strong gradient in the volumetric charge carrier densities, resulting in the diffusion of majority charge carriers into the oppositely doped region, as described by Eq. 2.2. Because holes and electrons are diffusing in opposite directions, a positive net current flows from the p-type region to the n-type region. This continues until enough positive charge develops in the n-type region near the boundary, and enough negative charge develops in the p-type region near the boundary that the resulting electric field prevents further diffusion, and the net current density becomes zero. The region near to the junction with non-zero

charge density is called the depletion region because the diffusion of minority charge carriers into the region leads to recombination and depletion of charge carriers. Fig. 2.4 illustrates the charge density distribution around a *pn* junction.

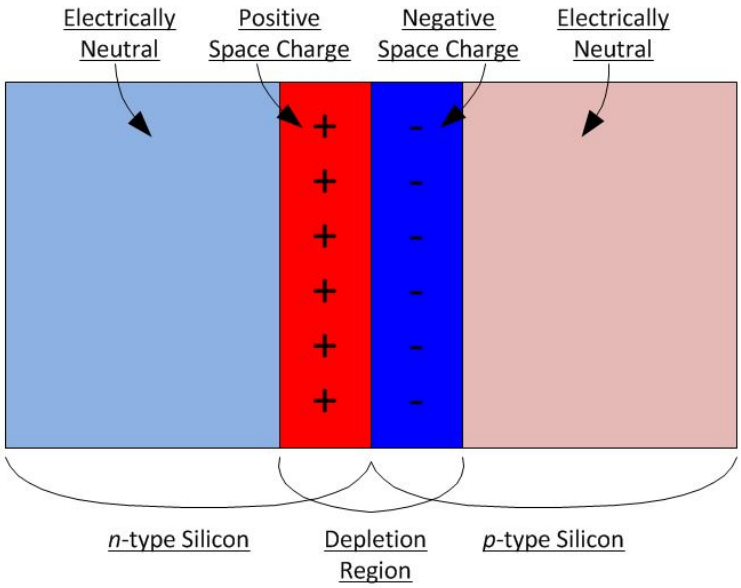

Figure 2.4: Charge density in *pn* depletion region.

The definition of the electric potential is given in Eq. 2.9.

$$V = -\int \vec{\boldsymbol{E}} \cdot d\vec{\boldsymbol{\ell}} \tag{2.9}$$

The polarized space charge that develops in the depletion region gives rise to what is known as the barrier voltage. Under open-circuited conditions, the n-type region rests at a higher potential than the p-type region, as given in Eq. 2.10. At 300 K, with typical doping concentrations, the barrier voltage for silicon is usually between 0.6 V and 0.8 V.

$$V_0 = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{2.10}$$

The barrier voltage is not observed at the terminals of the device, due to equal and opposite contact voltages that exists at the interface between the semiconductor and the metallic contacts.

In addition to the barrier voltage, the polarized space charge that develops in the depletion region results in a capacitance associated with the junction. Externally applied voltages may increase or decrease the charge bound in the depletion region in a nonlinear manner so that the capacitance associated with the junction is a function of both doping parameters and the applied external voltage, given in Eq. 2.11

$$C_{pn} = \frac{C_{pn,0}}{\left(1 + \frac{V_R}{V_0}\right)^m} \tag{2.11}$$

Here, m is the grading coefficient, which describes the manner in which the doping concentrations change across the junction. V_0 is the barrier voltage, given in Eq. 2.10, and V_R is the externally applied voltage, where the n-type region is held at a positive potential relative to the p-type region. $C_{pn,0}$ is the capacitance associated with the junction when no external voltage is applied.

$$C_{pn,0} = A\sqrt{\left(\frac{2\epsilon_{\mathrm{Si}} q_e}{2}\right)\left(\frac{N_p N_n}{N_p + N_n}\right)\left(\frac{1}{V_0}\right)} \tag{2.12}$$

Here, ϵ_{Si} is the electrical permittivity of silicon (1.04×10^{-12}), q_e is the elementary charge, N_p and N_n are the doping concentrations of the p-type region and n-type region, respectively, and V_0 is the barrier voltage.

2.1.4 Biased Junctions

The junction is considered to be forward biased when an external voltage is applied such that the p-type region is at a higher potential than the n-type region. If the externally applied voltage is less than the barrier voltage, the depletion region will diminish, but not disappear, and will block injection of charge carriers across the junction. If the externally applied voltage is greater than the barrier voltage, holes will be injected across the junction and into the n-type region, and free electrons will be injected into the p-type region. This high concentration of excess minority charge carriers near to the junction results in diffusion of excess minority charge carriers away from the junction. Minority charge carriers quickly recombine as they diffuse, and new majority charge carriers are supplied at the junction terminals to replace the loss of recombined charge carriers.

The junction is reverse biased when an external voltage is applied such that the p-type region is held at a lower potential than the n-type region. Under these conditions, electrons are taken out of the n-type region at the terminal, and holes are taken out of the p-type region at the opposite terminal. This decrease in majority carriers results in an increased bound charge in the depletion region, preventing significant current from flowing.

The *pn* junction is characterized by a reverse breakdown voltage V_{ZK}, that if exceeded, will result in significant current increase through a reverse-biased junction. Reverse breakdown may occur due to the Zener Effect, in which the electric field in the depletion region becomes strong enough to break covalent bonds and generate electron/hole pairs, or avalanche breakdown, in which free electrons gain sufficient kinetic energy from the electric field to ionize atoms upon impact [11].

2.1.5 Bipolar Junction Transistors

The bipolar junction transistor (BJT) is one of the most significant developments in semiconductor technology [12], with far reaching effects in virtually every modern industry. BJTs are three-terminal devices consisting of three doped semiconductor regions, forming two *pn* junctions. There are complementary types of BJTs, depending on the doping of the semiconductor: *npn* transistors and *pnp* transistors. Fig. 2.5 and Fig. 2.6 show the basic structure and circuit symbol for both types of transistors. The principles of operation are similar for both types, so only *npn* operation is detailed here.

The device possesses three terminals, each connected to one of the three semiconductor regions: the collector, the base, and the emitter. The device's operation is considered for the circuit shown in Fig. 2.7.

Voltage source "V_BE" forward biases the base-emitter junction, causing current to flow. Holes are injected from the base into the emitter, and electrons are injected from the emitter into the base.

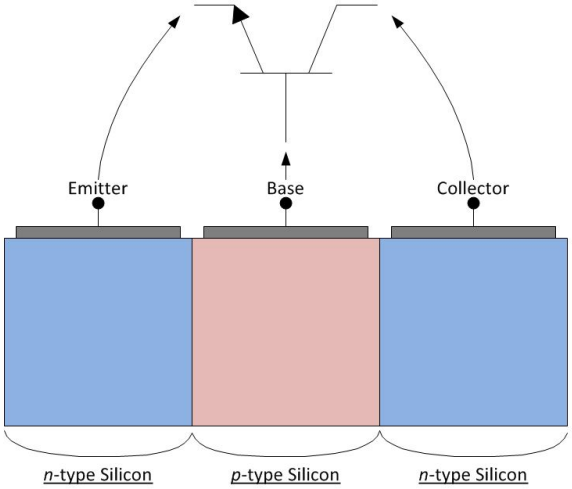

Figure 2.5: Structure and symbol of an *npn* transistor.

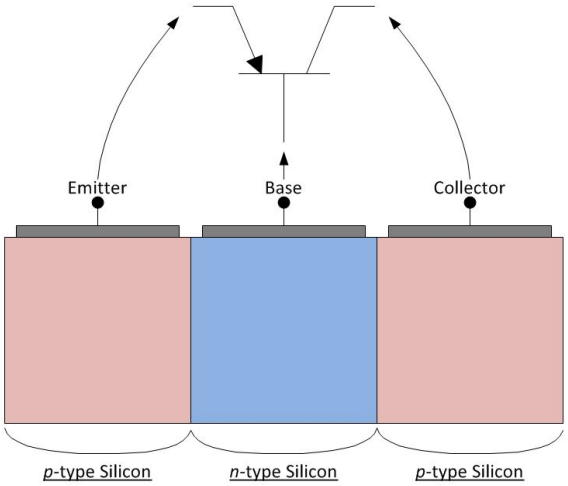

Figure 2.6: Structure and symbol of a *pnp* transistor.

In physical devices, the geometry and doping of the emitter and base regions are important. Real devices usually possess heavily doped emitters and lightly doped bases so that electron flow from the emitter to the base is the dominating component of the current through the junction. This leads to a high population density of electrons at the base-emitter junction, resulting in the diffusion of electrons into the volume of the base. Since the base is lightly doped, few of the injected electrons recombine.

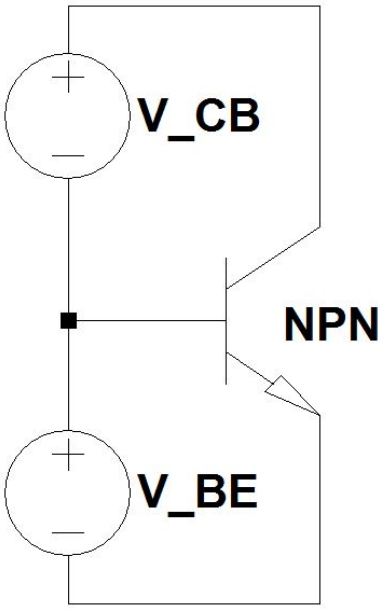

Figure 2.7: Simple transistor biasing schematic.

Because the base-collector junction is reverse biased, an electric field is present in the depletion region. Diffusing electrons in the base that reach the base-collector junction are immediately swept into the collector by this electric field, resulting in positive current flow from the collector region into the base region.

This process gives rise to a high current gain, so that collector current is a function of the base current, as given in Eq. 2.13

$$i_C = \beta i_B \tag{2.13}$$

If i_B become great enough, the collector current may approach the current-sourcing capabilities of voltage source "V_CB". In this event, the biasing of the transistor may change so that the collector-base junction is no longer reverse biased. In this event, the transistor becomes saturated, and the current gain β will decrease.

Transistors used as switches are typically operated in the cutoff regime, where $i_B = 0$, or the saturation regime, where i_B is great enough to saturate the transistor.

2.2 Thyristor-Type Switches

A thyristor, or silicon-controlled rectifier (SCR), is a bistable, three-terminal semiconductor switch. The high voltage hold-off and current conduction capabilities of thyristor-type switches set them apart from other classes of semiconductor switches [14]. As semiconductor design and fabrication technology has matured, thyristors have become viable replacements for gas discharge switches [15]. Silicon Power, Inc. has developed a thyristor capable of holding off 4 kV and switching 14 kA [1].

2.2.1 Device Structure

The thyristor's terminals are anode, gate, and cathode, and it consists of four doped regions, as shown in Fig. 2.8.

The anode and cathode terminals function as the switch terminals, blocking high voltage in the off state and conducting high current in the on state. The gate terminal is used to trigger the device. The behavior of the *pn* junctions is best understood by considering the thyristor to be two bipolar junction transistors, one *npn* and one *pnp*, connected as shown in Fig. 2.8.

2.2.2 Switching Behavior

It can be seen that if the current flowing into the gate terminal is zero, the lower *npn* transistor will be off, and will have collector current of 0 A. As a result, no

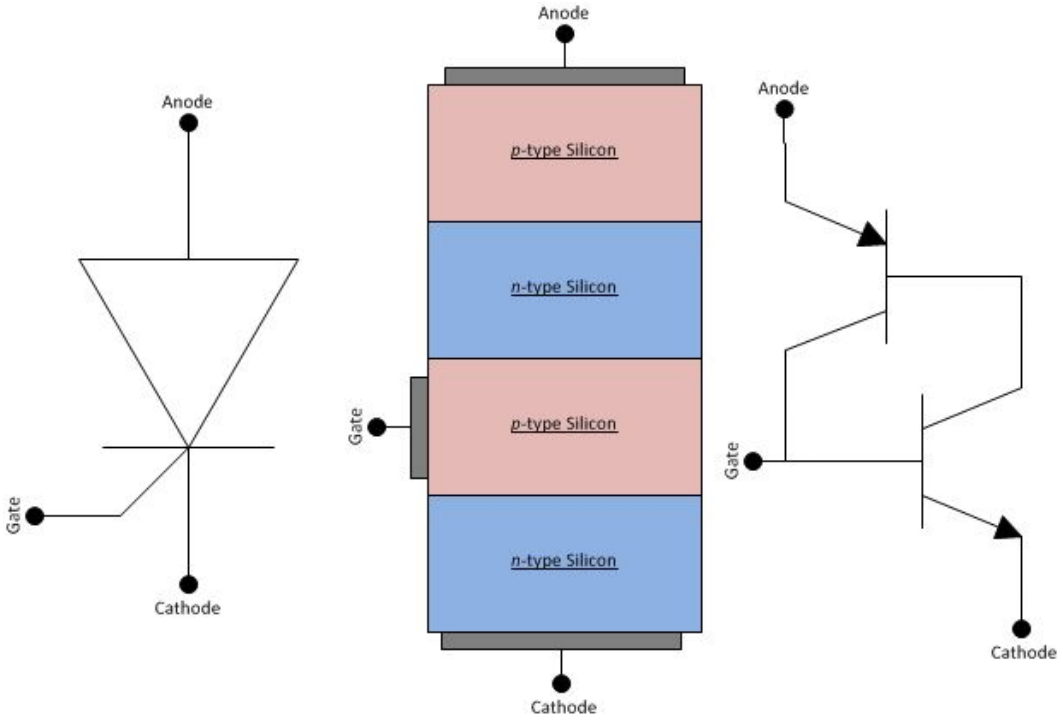

Figure 2.8: Thyristor symbol, structure, and equivalent transistor circuit.

current will flow out of the base of the upper *pnp* transistor, also ensuring that it conducts no current.

In the presence of a voltage drop from the anode to the cathode, if a sufficient current i_G (specified in the manufacturer's data sheet) is injected into the gate terminal (or equivalently, the base terminal of the lower *npn* transistor), the lower *npn* transistor will begin to conduct a collector current, which will be equal to the base current experienced by the upper *pnp* transistor. The upper transistor will then begin to conduct an emitter current, and the base current of the lower *npn* transistor then becomes $i_{B,npn} = i_G + i_{E,php}$. This then results in an increased collector current in the lower *npn* transistor according to it's gain parameter β. This increased collector current in the lower transistor is experienced as a base current in the upper tran-

sistor, which then begins to conduct a greater emitter current. It is seen that this positive feedback continues until both transistors are saturated and fully on. As long as a positive current continues to flow from the anode to the cathode, the device will remain on, and cannot be turned off. Recently, a special class of thyristors, called gate-turn-off (GTO) thyristors, have been developed that can be turned off by driving positive current out of the gate terminal, but normal thyristors, such as the one of interest in this thesis, do not possess this feature.

Of particular interest here is the transient behavior of the thyristor as it transitions from off to on. Initially, the charge carrier density at any given location in the device is simply the doping concentration plus the thermally generated charge carrier density, with some redistribution of charge due to the diffusion of charge carriers, as discussed previously. A more realistic device structure is shown in Fig. 2.9.

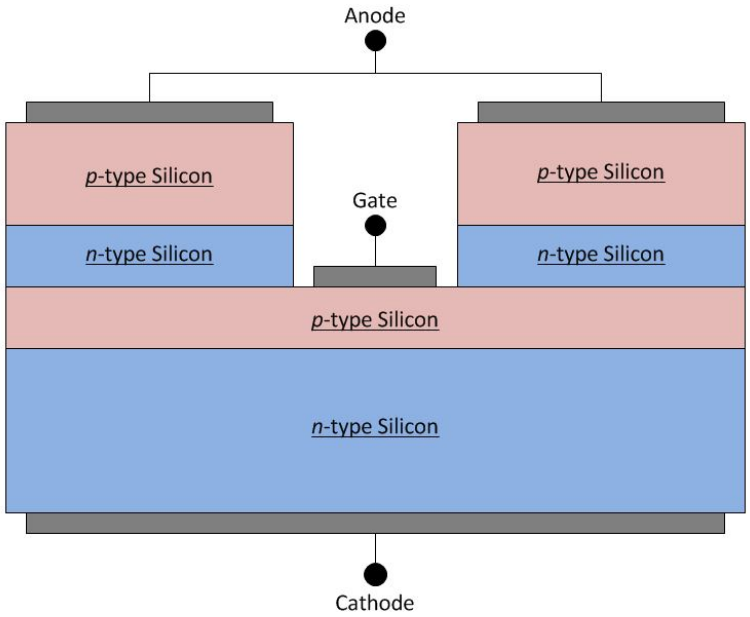

Figure 2.9: A more realistic example thyristor structure.

When the triggering current pulse is driven from the gate to the cathode, the entire cross-section of the device does not turn on instantaneously. Initially, only the region immediately surrounding the gate contact develops a significant charge carrier density and conducts current. As the positive feedback process of turn-on progresses, charge carriers diffuse away from the gate and turn on a greater cross-section of the device, until the entire cross-section is conducting current. This diffusion of charge carriers throughout the device cross-section is known as plasma spread.

Plasma spread limits the rate at which the current through the device can increase without risking damage. If the current through the switch increases to an extremely high value while only a small portion of the cross-section is turned on, the current density in the region that is turned on may exceed the capabilities of the device. The maximum rate at which current can safely be increased is usually specified in the manufacturer's data sheet. For the CCS-SC-14N40, the maximum dI/dt is specified as $30\,\mathrm{kA/\mu s}$, placing it's maximum dI/dt far above most thyristor switches, which are typically rated for a maximum dI/dt on the order of a few hundred $\mathrm{A/\mu s}$.

Because switching is triggered by driving a current through the gate-cathode pn junction, the switch can only sustain a finite rate of increase of voltage between the anode and cathode. A reverse biased pn junction just above the gate region holds off the anode-cathode voltage, and possesses an associated capacitance. In the event of a rapidly increasing voltage across the junction, some current will flow. Kirchoff's current law dictates that that current must also pass through the gate-cathode pn junction, and if the current is of sufficient magnitude, the device may turn on.

The maximum dV/dt that can be sustained without triggering the device is specified in the manufacturer's data sheet. Silicon Power's CCS-SC-14N40 is specified to be able to withstand up to 1 kV/µs. The risk of unintentionally triggering can be minimized by placing a low-value resistor between the gate and cathode terminals of the switch to divert current away from the gate-cathode *pn* junction. The data sheet for the CCS-SC-14N40 suggests 10 Ω.

2.2.3 Current-Voltage Characteristics

An example thyristor IV curve is shown in Fig. 2.10.

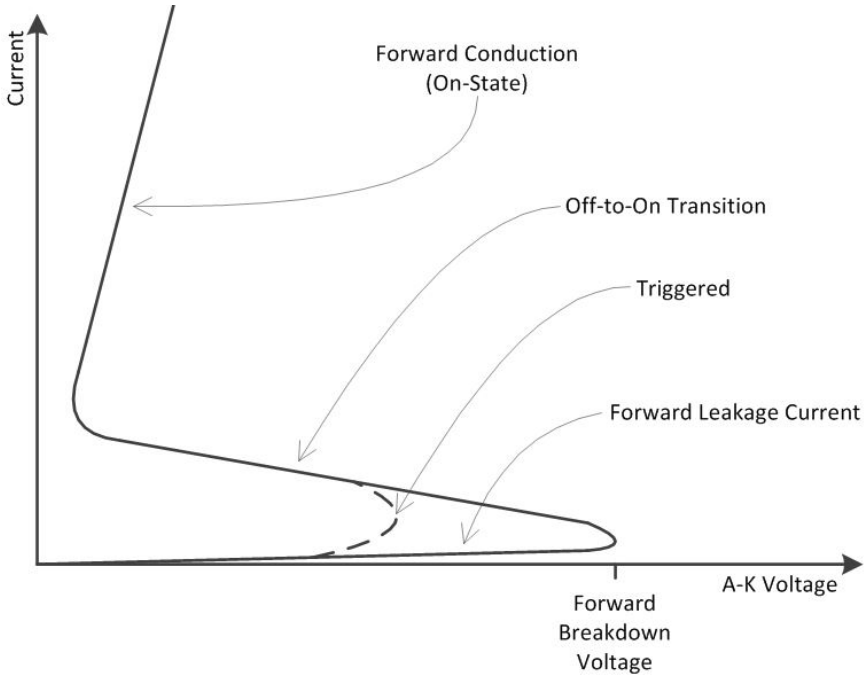

Figure 2.10: Generic thyristor current-voltage curve.

The device is considered to begin in the off state. As the anode to cathode voltage increases, a very small leakage current begins to flow through the device. The leakage current is usually in the µA range and is not sufficient to turn on the switch.

If the device is triggered by driving a sufficient current into the gate, the current through the switch increases as the voltage across the switch collapses, and the device enters the forward conducting regime, which is characterized by high dI/dV.

Thyristors can only sustain a certain voltage drop across the switch before the reverse biased *pn* junction breaks down, resulting in device turn-on. The maximum hold off voltage is referred to as the forward breakdown voltage, and is specified in the manufacturer's data sheet.

2.2.4 Device Turn-Off

Once a thyristor has turned on, it will remain on as long as it experiences a sustained forward current. When current decreases below a threshold value, or reverses polarity, minority charge carriers begin to recombine in the semiconductor. The recombination of charge carriers may take tens or hundreds of µs to achieve a sufficiently low minority charge carrier density for the device to begin blocking forward current conduction. For this reason, a thyristor may experience a ringing current that continues for many periods of oscillation if the the current polarity is not reversed for a sufficient time for the device to turn off. This behavior limits the repetition frequency of the switch in repetitively pulsed applications.

2.2.5 CCS-SC-14N40 Specifications

Maximum ratings and performance specifications given by the manufacturer are shown in Table 2.2.

2.3 Existing Models

There are currently many available models for simulating the behavior of thyristors. This thesis is concerned with a novel technique for thyristor modeling that is implementable in a SPICE circuit simulation software, and accurately models the transient switching behavior of the device.

Existing models that are convenient to implement in a SPICE simulation tend to neglect the switching behavior of the device, and only model the basic characteristics of device operation, such as an indefinite forward current conduction, forward breakdown voltage, and time-delayed turn-off in the event of current below a threshold value [2].

Other modeling techniques achieve a high degree of fidelity, but are extremely difficult to obtain for a particular device, and are not convenient to implement in a SPICE simulation. One model in particular [3] achieves excellent agreement with experimentally measured device behavior, but requires knowledge of the semiconductor's geometry and doping profiles, which is proprietary information for most devices. Furthermore, this information is to be used with an advanced semiconductor simulation software package to extract parameters to be used in constructing a model based on two transistors, which are each implemented via the Gummel-Poon model [13].

Another model that is convenient to implement in SPICE and is accurate in transient switching analysis is a function of discharge parameters. That is, if the capacitance, load, or stray inductance changes, the model must be adjusted accordingly [5].

Table 2.2: CCS-SC-14N40 Maximum Ratings and Performance Specifications

Parameter	Value
Peak Off-State Voltage	4 kV
Peak Reverse Voltage	−5 V
Off-Stage dV/dt Immunity	1 kV/µs
Continuous Anode Current	100 A
Repetitive Pulsed Peak Anode Current	10 kA
Single-shot Pulsed Peak Anode Current	14 kA
Peak dI/dt	30 kA/µs
Peak Gate Current	100 A
Peak Reverse Gate-Cathode Voltage	−9 V
Peak Junction Temperature	125 °C
Leakage Current	<50 µA
Turn-On Current Threshold	5 mA
Turn-On Delay Time	200 ns

CHAPTER 3

EXPERIMENTAL SETUP

In order to characterize the behavior of Silicon Power's CCS-SC-14N40, voltage vs. time and current vs time waveforms are recorded. Special consideration is given to the driving circuit to safely operate at high voltages, high pulsed currents, and high dI/dt with minimal risk of damaging equipment. Furthermore, special measurement tools were used to accurately measure fast, transient, high voltage/current pulses.

3.1 Experimental Circuit

The simplified experimental circuit schematic is shown in Fig. 3.1.

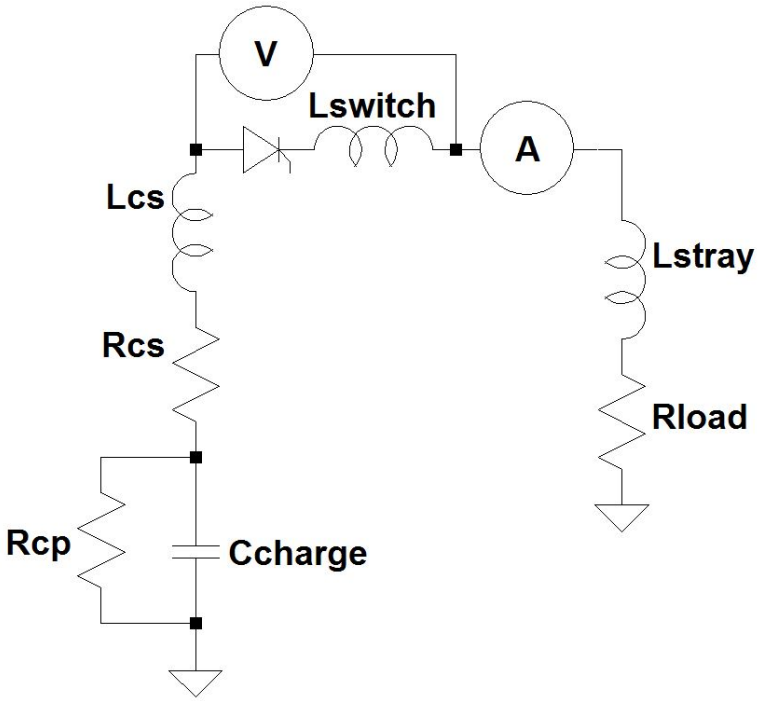

Figure 3.1: Simplified Experimental Circuit Schematic. "V" represents a voltage probe and "A" represents a current monitor. Parasitics are included.

The schematic depicts a capacitor Ccharge, that is charged to some voltage V_0 and is discharged into a load resistance Rload. Several important parasitic components are shown in the schematic. First, the capacitor possesses some series resistance Rcs, as well as a series inductance Lcs, which adds to the total series resistance and inductance of the circuit. Second, the metal conductors that connect the circuit components possess an inductance L_{stray} that affects the behavior of the circuit. A final addition to the total circuit inductance is the inductance associated with the switch itself, Lswitch. These elements are important to consider in obtaining and verifying the model, since the model's accuracy should be as independent as possible from the characteristics of the circuit in which it is used. There is a parasitic resistance Rcp in the capacitor that has the effect of bleeding off charge in the capacitor. This parasitic resistance is very large, affects performance on very long time scales, and is therefore neglected in the evaluation of the circuit's performance. In experiments, the total series inductance was measured to be roughly 187 nH.

The thyristor is packaged as shown in Fig. 3.2.

The package features eight connections: two for the anode, two for the gate, and four for the cathode. The device is connected to a printed circuit board by cutting rectangular holes so that the tabs of the package can be inserted and soldered to surface-mount pads, which are located at the edges of the rectangular holes.

The experimental circuit is constructed on a printed circuit board. The experimental circuit schematic is shown in Fig. 3.3, and the PCB layout is shown in Fig. 3.4.

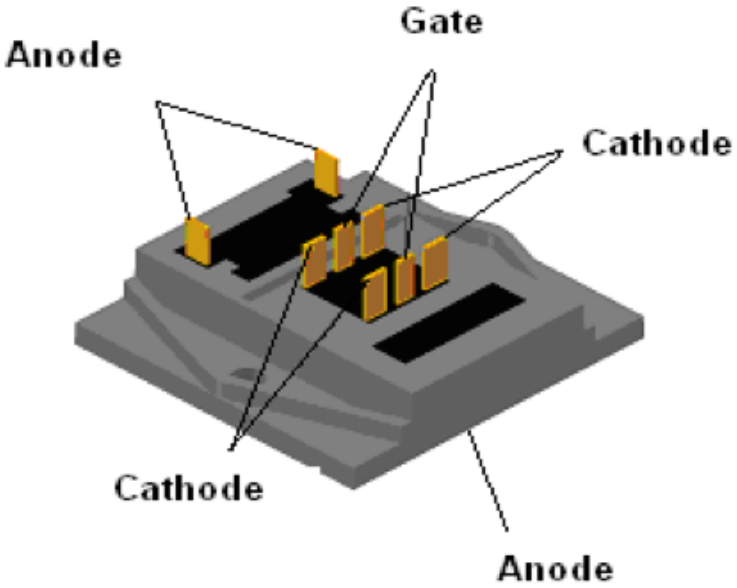

Figure 3.2: Silicon Power's CCS-SC-14N40 package. Package dimensions are 1.417" × 1.357" × 0.495".

3.1.1 High Voltage/Current Discharge Circuit

The thyristor is configured as a high-side switch, that is, it is connected between the high-voltage capacitor terminal and the load. Vias located directly beside the anode and cathode terminals of the switch enable a small loop of bare wire to extend above the surface of the board, to which a high-voltage differential probe is connected, shown in Fig. 3.5. The vias are intentionally placed in close proximity to the anode and cathode to minimize any additional stray inductance between the point of measurement and the switch terminals that might affect the voltage measurements in high dI/dt discharges. A CIC Research DP03-1K-50 high voltage differential probe is used to measure the voltage across the switch. The probe supplies a 1000:1 proportional voltage to a 50 Ω load, and has a specified bandwidth of 75 MHz for measurement of rise and fall times as low as 4 ns.

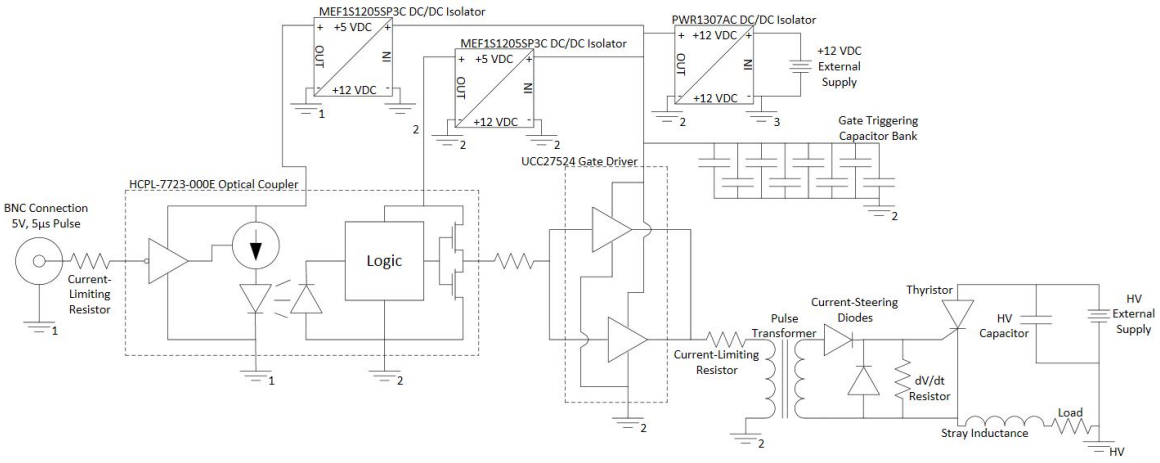

Figure 3.3: Experimental Circuit Schematic. The board features 4 isolated ground references, indicated by numbers 1-3 and HV for the high voltage discharge circuit ground.

Ten resistor connections are placed in parallel to minimize the inductance of the load, as well as to enable energy to be deposited among several components. In the event that an extremely small load is needed, several carbon composition resistors can be clamped together in parallel using a c-clamp and metal plates, as shown in Fig. 3.6.

For discharges into a shorted load, metal wire is used to directly short-circuit all ten resistor spaces, to minimize the ohmic losses in the wire and to minimize the additional stray inductance.

High voltage capacitors are either connected directly to the capacitor terminals at the lower-right corner of Fig. 3.4, or for capacitances above 4.7 nF, capacitors are connected via screws and bolts to high-voltage rated wires that extend from the capacitor terminals, as shown in Fig. 3.7.

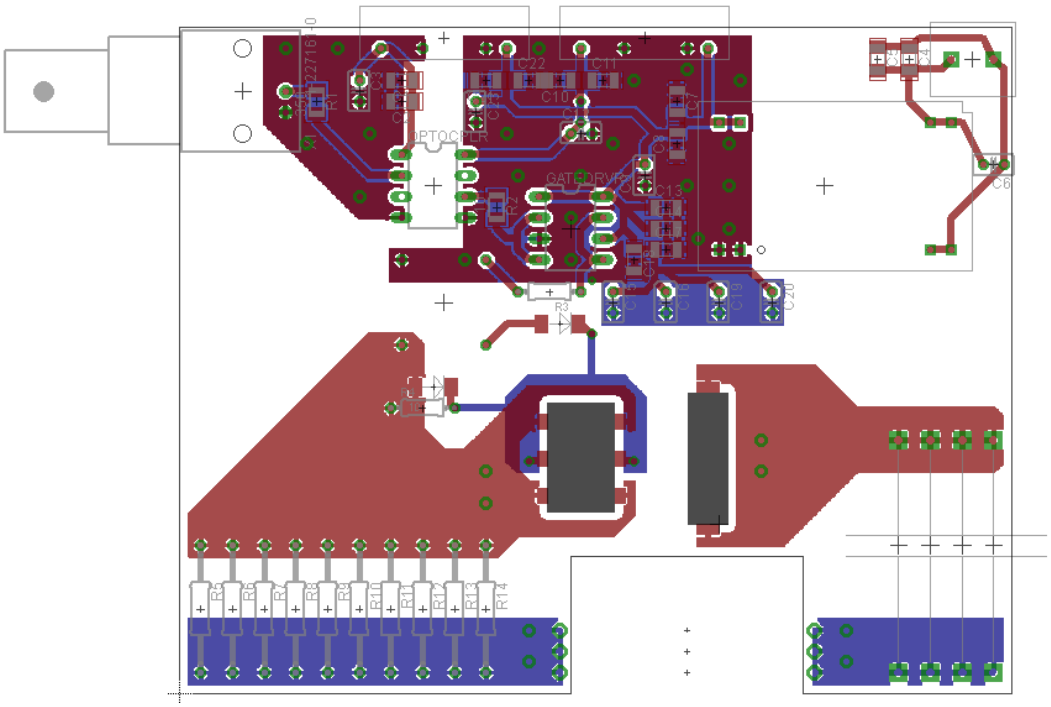

Figure 3.4: Experimental Circuit Printed Circuit Board Layout. Board dimensions are 3.125" × 4".

A Pearson 5046 current monitor is placed on the 0 V wire connecting the capacitors to the circuit, also shown in Fig. 3.7. The current monitor supplies a voltage proportional to the current passing through it's center. Here, 0.01 V/A is supplied into a open circuit load with a 50 Ω output impedance. For driving a 50 Ω oscilloscope load, 0.005 V/A is measured.

3.1.2 Triggering Circuit

The switch is triggered by applying a 5 V, 5 µs pulse to the BNC connection located at the top-left of Fig. 3.4. The trigger signal drives a current through a current-limiting resistor and a light emitting diode located in the input terminal of a Fairchild Semiconductor FOD3182 optical coupler IC, which provides high voltage isolation

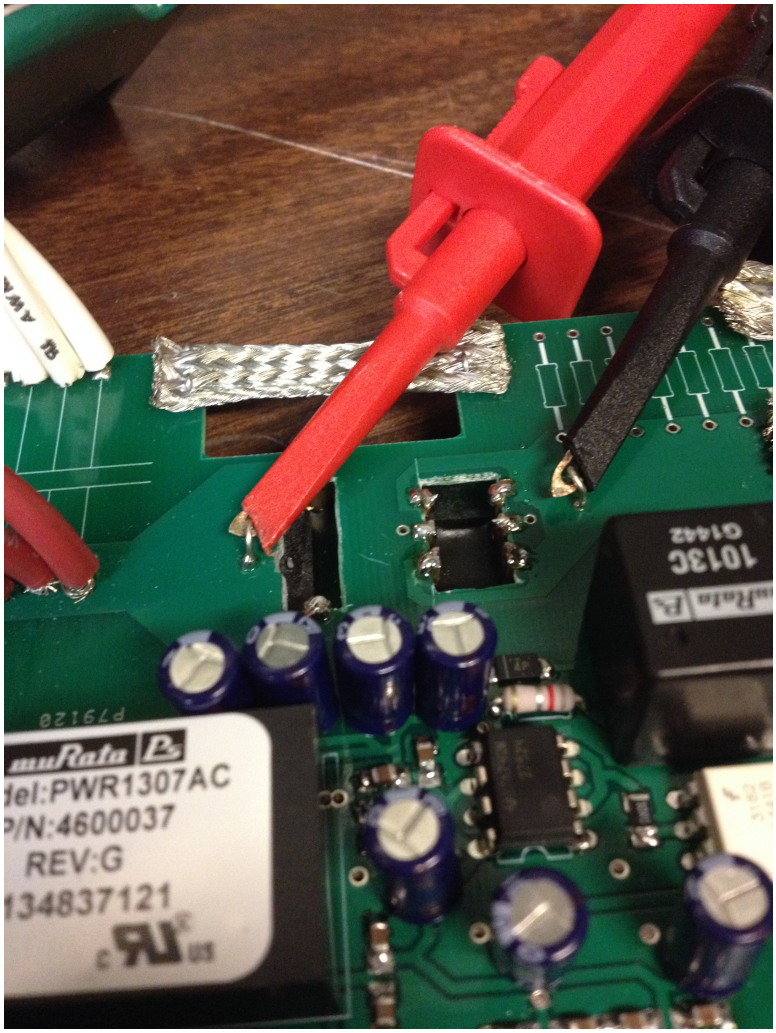

Figure 3.5: High-voltage differential probe connections on the experimental PCB.

between the gate-driving circuitry and the trigger signal generator, which may be EMI sensitive. The optical coupler IC delivers the signal at 12 V to the logic inputs of a Texas Instrument gate driver IC. A capacitor bank of ceramic capacitors and electrolytic capacitors connected in parallel provide a low-impedance source capable of driving a fast rise time, 10 A pulsed current through a 1.2 Ω current-limiting resistor and into the primary terminals of a 1:1 pulse transformer, which provides further high-voltage isolation between high voltage/current pulses and other connected circuitry.

Figure 3.6: Carbon composition resistors used for low impedance loads. The configuration here is measured to be 0.3 Ω. The C-clamp is isolated from the top plate by multiple layers of kapton tape.

The gate-driving capacitor bank consists of multiple ceramic capacitors, which feature low series resistance and inductance to enable fast transient current sourcing, and larger electrolytic capacitors which are capable of storing more charge, allowing for longer current pulses without deteriorating voltage. The pulse transformer is selected for minimum leakage inductance (3 µH and sufficient core size to withstand at least 60 V µs (12 V, 5 µs pulse).

The pulse transformer couples current into a network of current-steering diodes and into the gate terminal of the thyristor. The diodes prevent significant voltage from being applied across the secondary terminals when reverse current flows through

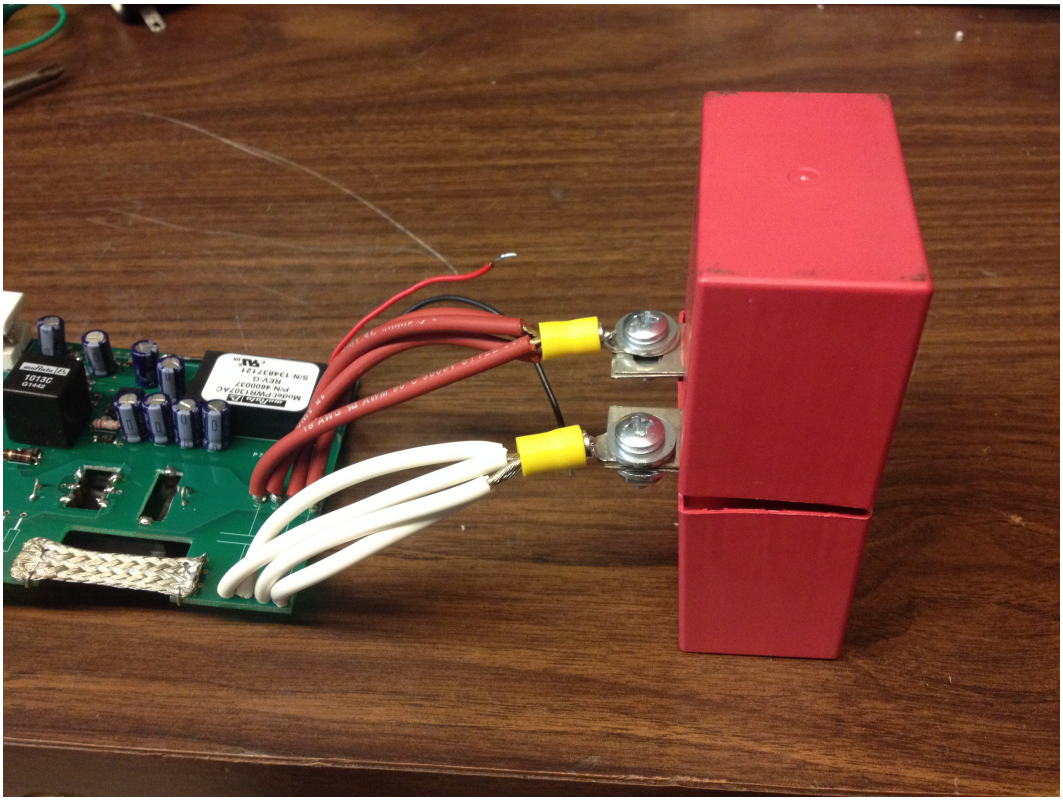

Figure 3.7: Two 330 nF capacitors connected in parallel to the experimental PCB.

the thyristor by providing a forward-biased *pn* junction for current conduction from the thyristor cathode to the gate. Because the *pn* junction between the gate and cathode is forward biased during forward current conduction, a signifiant voltage will not develop across the secondary terminals during forward current conduction.

A 10 Ω resistor is connected between the gate and the cathode of the thyristor, creating a current path that bypasses the gate-cathode *pn* junction. This is necessary because during charging of the HV capacitors, the capacitance associated with the reverse-biased *pn* junction in the thyristor allows for current to flow through the switch as the voltage across the switch increases. This current may be enough to trigger the switch if the anode-cathode voltage increases too quickly, but the effect

can be minimized by diverting current away from the gate-cathode junction through a parallel resistor.

3.1.3 Triggering Circuit Power Supply

The gate driving circuit is powered by a 12 V DC source. The source is isolated from the gate driving circuit by a Murata PWR1307AC 12 V/12 V DC/DC isolator rated for 1 W. DC/DC Isolators are important devices in systems that involve interfacing between low power and high pulsed power systems. Decoupling capacitors are placed in close proximity to the input and output connections of the isolator to minimize EMI that might couple backward through the isolator and into the source. Additionally, isolated ground planes are separated as much as possible to minimize the capacitance between the two ground planes, further reducing the possibility of EMI coupling back into the source.

3.1.4 High Voltage Charging Supply

An adjustable Ultravolt BT-GP series 10 kV, 3 mA high voltage DC power supply is used to charge the capacitor bank to a desired voltage equal to or less than 4 kV through a 4 MΩ charging resistor. Because the high voltage differential probe used to measure the transient voltage across the thyristor has a finite input impedance between the terminals, a significant current leaks through the probe. The result is that the voltage supplied by the high voltage source is divided between the charging resistor and the differential probe, so that the voltage on the capacitors must be

directly measured using a DC high voltage probe connected to a digital multimeter. The high voltage supply is then adjusted until the desired voltage on the capacitors is measured.

Voltage and current waveforms are recorded on a 4 GSa/sec Agilent Infinium 54832D MSO oscilloscope.

CHAPTER 4

MODEL DETERMINATION

Voltage across the thyristor vs time and current vs time measurements are recorded for various charging voltages, capacitances, and loads. A typical waveform is shown in Fig. 4.1.

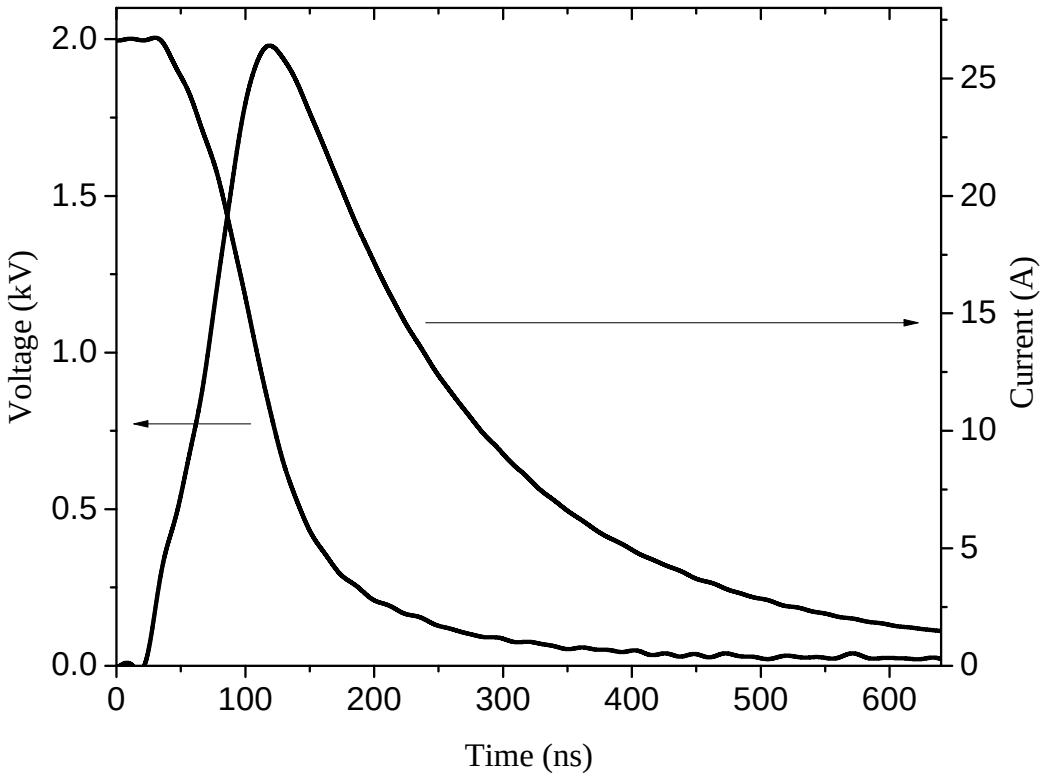

Figure 4.1: Current through the switch and voltage across the switch vs time waveforms for 3 nF charged to 2 kV discharged into 20 Ω. Arrows indicate axis association.

In Fig. 4.1, the voltage across the switch is initially 2 kV, and the current through the switch is 0 A, indicating that the switch is in the off state. After the switch is triggered and begins conducting current, the current through the switch begins to rise

as the voltage across the switch falls. As the switch becomes increasingly conductive, the current waveform becomes dominated by external circuit parameters such as the load resistance and total series inductance in the circuit. In Fig. 4.1, the current waveform assumes the shape of an exponential RC decay after the switch closes. The low voltage across the switch and non-zero current toward the end of the waveform indicated that the switch has closed, and is behaving as a conductor.

4.1 Equivalent Switch Resistance

The switch is modeled as a dynamic resistance, where the resistance is a function of the instantaneous current through the device and the total charge that has passed through the device.

For purposes of the switch model presented here, the equivalent resistance of the switch is defined as the ratio of the voltage across the switch to the current through the switch. For low current pulses, the rate of change of the current is considered to be sufficiently small so that $L_{thy}\frac{di}{dt} << V_{thy}$, where L_{thy} is the internal switch inductance and V_{thy} is the voltage across the switch. In this case, the equivalent resistance of the switch reduces to the ratio of voltage to current, shown in Eq. 4.1

$$R_{thy} = \frac{V_{Thy}}{I_{Thy}} \tag{4.1}$$

After adjusting for time delays in the voltage and current waveforms that arise from differences in coaxial transmission line length between diagnostic probes and the oscilloscope, the equivalent switch resistance is calculated by dividing the voltage

by the current waveform, point-by-point. An example resistance vs time waveform is plotted in Fig. 4.2.

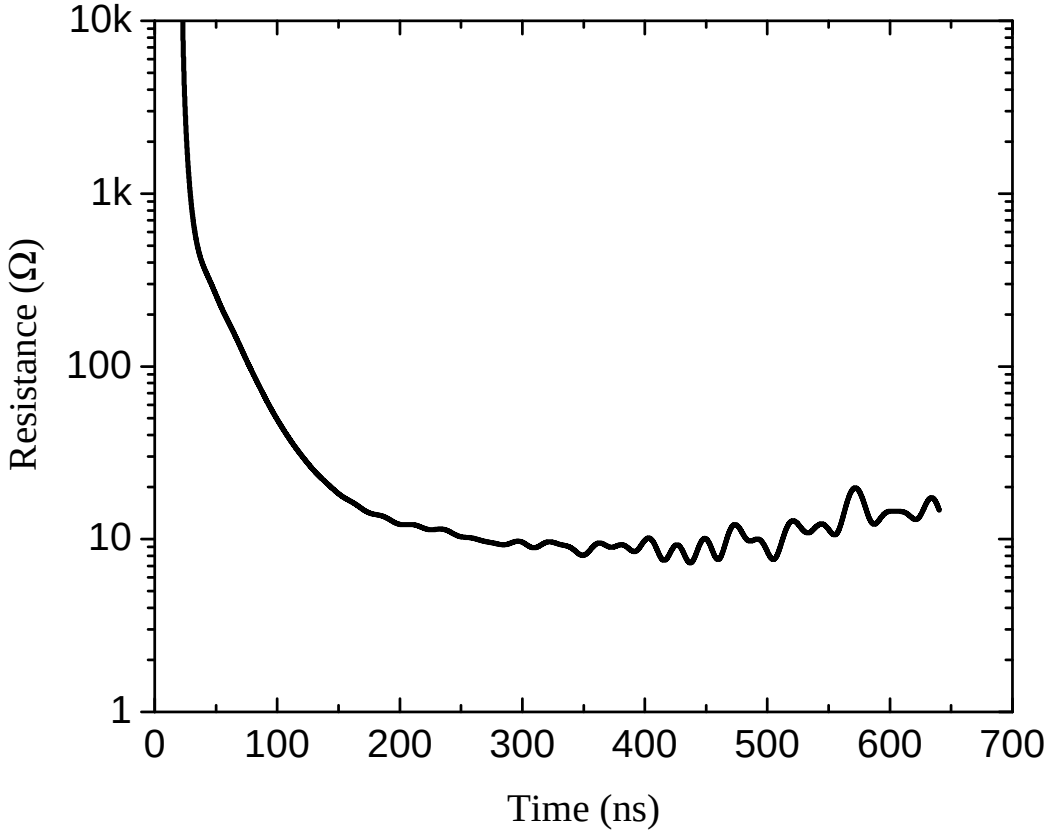

Figure 4.2: Equivalent switch resistance vs time waveform for 3 nF charged to 2 kV discharged into 20 Ω.

In Fig. 4.2, the the switch is in the off state from 0 ns to 25 ns, as indicated by it's extremely high resistance. Once triggered, the switch resistance rapidly drops and reaches a minimum of around 10 Ω at roughly 250 ns after switching.

4.1.1 Resistance vs Current and Charge

As previously mentioned, the thyristor transitions from the off state to the on state as an increasing cross-section of the device turns on and begins conducting current.

This processes occurs more quickly if more charge is being injected into the device. It is therefore expected that a relationship may exists between the equivalent switch resistance, the instantaneous current, and the total charge that has passed through the switch. Fig. 4.3 plots the equivalent switch resistance vs instantaneous current.

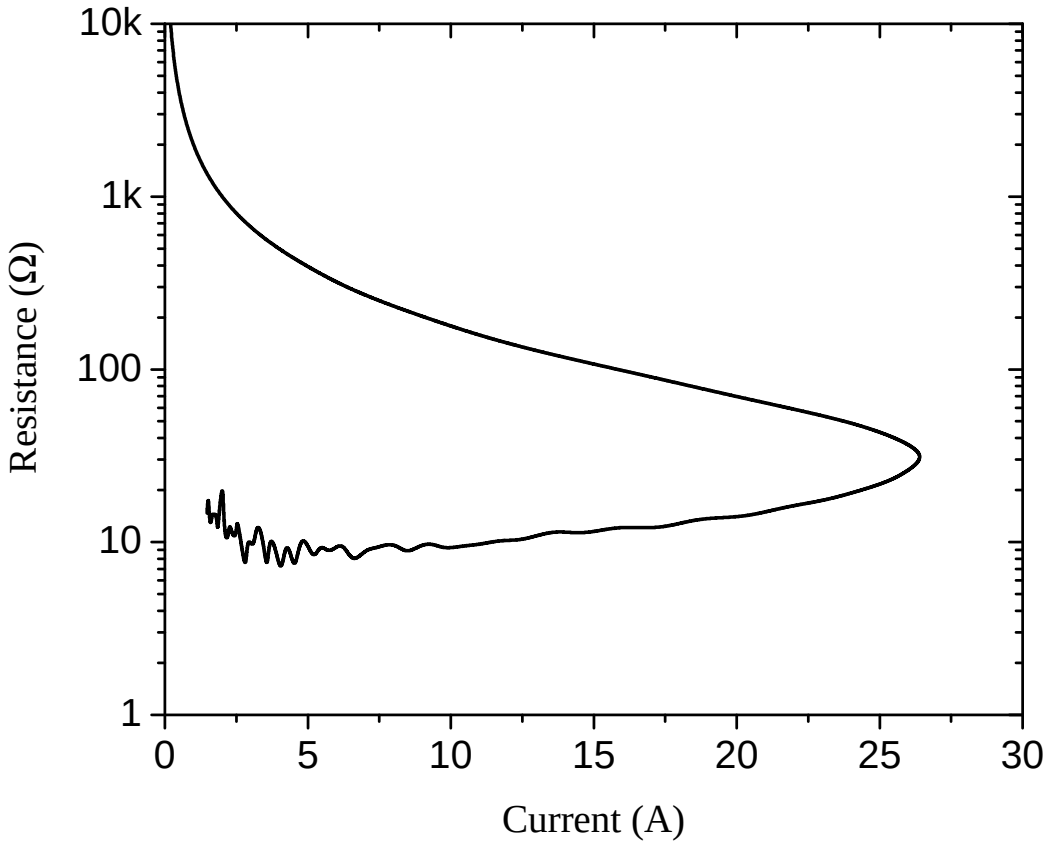

Figure 4.3: Equivalent switch resistance vs instantaneous current for 3 nF charged to 2 kV, discharged into 20 Ω.

The transition from the off state to the on state can be observed in Fig. 4.3. Initially, the switch is in the off state, exhibiting very high resistance and conducting almost zero current, placing the switch on the vertical axis and above the range of the plot. As the switch transition from off to on, the resistance quickly drops as the current simultaneously increases, until the peak current is achieved. As time

continues, the capacitor that drives the current loses charge, resulting in a decrease in current. Although the current decreases, the switch resistance remains low because the switch is still on.

The same transition is observed in Fig. 4.4, which plots the equivalent switch resistance vs total charge that has passed through the switch.

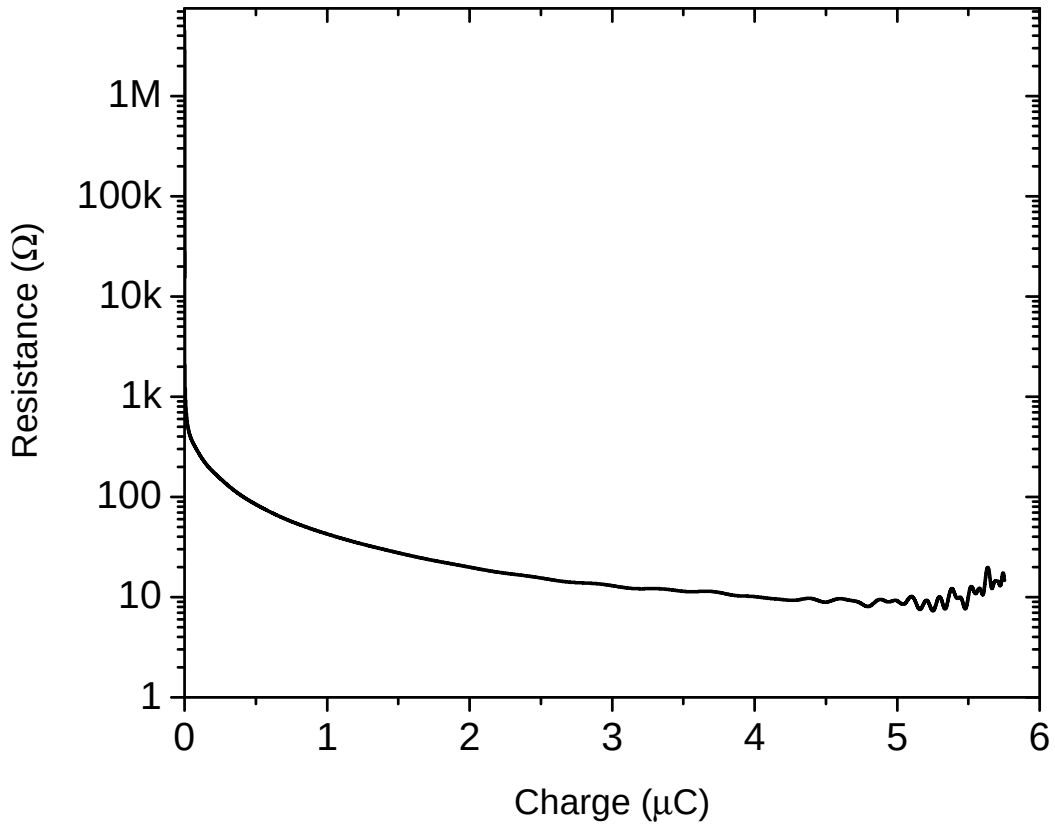

Figure 4.4: Equivalent switch resistance vs total charge conducted for 3 nF charged to 2 kV, discharged into 20 Ω.

Similar to Fig. 4.3, the transition from off to on is observed in Fig. 4.4 by the switch beginning on the vertical axis, indicating that no charge has passed through the switch, and above the vertical range of the plot, indicating the very high resistance associated with the off state. As the switch transitions from off to on, the equivalent

resistance rapidly drops as charge begins to pass through the switch. Although the current waveform moves back toward the vertical axis toward the end of the discharge, indicating the decaying current, the total charge does not decrease with time, since the current does not actually reverse polarity in this discharge.

The waveform shown in Fig. 4.3 is obtained by calculating the switch resistance via point-by-point division of the voltage by the current waveforms recorded by an oscilloscope, and plotting against the current observed at each corresponding point in time. The waveform shown in Fig. 4.4 is obtained similarly, except that the total conducted charge at any given point in time is calculated via trapezoidal approximation of the integral of the current waveform.

Although the relationship is not readily observed from the waveforms in Fig. 4.3 and Fig. 4.4, a relationship becomes apparent when the equivalent switch resistance is plotted vs instantaneous current and total charge conducted in a 3-D plot, shown in Fig. 4.5.

The various waveforms in Fig. 4.5 exhibit the same behavior as described for Fig. 4.3 and Fig. 4.4. The switch begins with a very high resistance, indicating that it is off. As the switch transitions, the resistance falls and both charge and current increase. As the discharge continues, current peaks and then begins to decline as charge continues to increase until the capacitor is discharged.

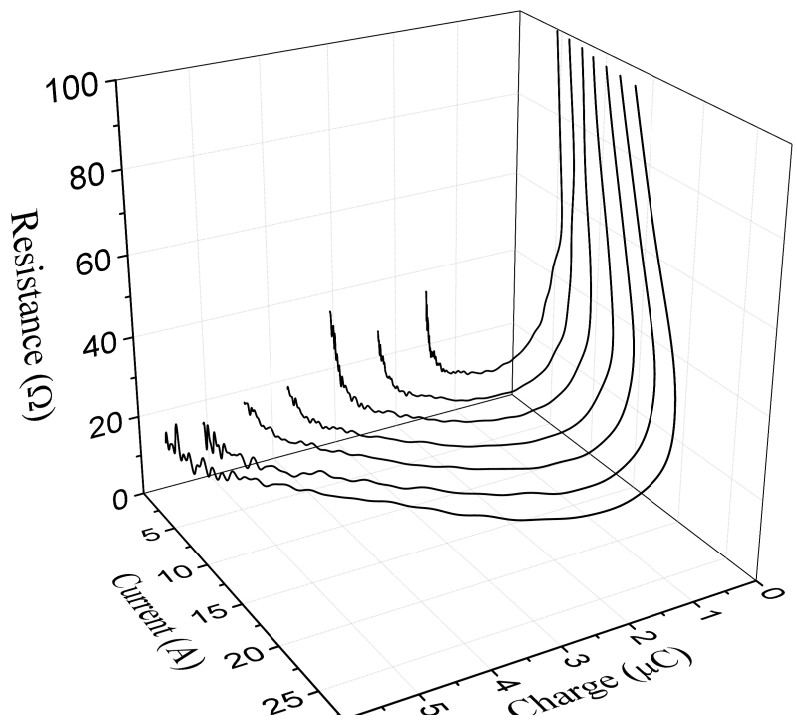

Figure 4.5: Equivalent switch resistance vs instantaneous current and total charge conducted for 3 nF charged to varying voltages, discharged into 20 Ω.

4.1.2 Empirical Formula Model

Examination of Fig. 4.5 suggests that a relationship exists between the equivalent switch resistance, the instantaneous current, and the conducted charge, as indicated by the surface that the waveforms all follow. The empirical formula in Eq. 4.2 is proposed to describe the surface traced by the waveforms.

$$R_{thy}\left(I, \int Idt\right) = \Bigg[C_1\left(\int Idt\right)^{C_2 I^{-C_3}+C_4} + C_5 e^{-(C_6 I + C_7 \int Idt} + C_8 I + C_9\Bigg] e^{-C_{10}\int Idt} \tag{4.2}$$

Here, R_{Thy} represents the model's estimation of the equivalent resistance of the switch, I represents the instantaneous current through the device at the moment at which resistance is calculated, and $\int Idt$ represents the total conducted charge that has passed through the switch up until the moment at which the resistance is calculated.

4.1.3 Model Optimization

Eq. 4.2 attempts to empirically describe the shape of the surface traced by the multiple waveforms in Fig. 4.5. Ten constant parameters C_1 - C_{10} are used to fit the formula to the observed data. Optimization is performed by minimizing the cost function in Eq. 4.3.

$$\boldsymbol{C_{best}} = \min_{\boldsymbol{C}} \left\{ \sum_{n=1}^{N} \frac{|R_{thy,n}(I, \int Idt) - R_n|}{R_n N} \right\} \tag{4.3}$$

Here, R_n refers to a single experimentally measured equivalent switch resistance data point. Depending on the time duration of the recorded waveforms and the sampling rate of the oscilloscope, there may be as many as 50,000 resistance data points per recorded waveform. N refers to the total number of experimentally observed resistance data points, which may include all the observed data points for multiple discharges. $R_{Thy,n}(I, \int Idt)$ refers to the formula given in Eq. 4.2, where the model resistance is calculated for the same instantaneous current I and conducted charge $\int Idt$ as the corresponding experimentally observed resistance data point. This expression gives the set of constant parameters C_1 - C_{10} that results in the minimum

average absolute error between the model resistance and any given observed resistance data point for an arbitrary number of waveforms each containing an arbitrary number of data points. Because data points corresponding to the off state may result in extremely high absolute error, this cost function may give disproportionate weight to data points of high resistance. For this reason, only data points below 100 Ω are considered for purposes of constant parameter selection.

A simple gradient descent algorithm is unsuitable due to the many local minima that exist in the cost function as a result of the high dimensionality of the parameter space (10 real dimensions). Therefore, a particle swarm optimization algorithm [16, 17] is implemented in massively paralleled fashion on a graphics processing unit to arrive at an optimal set of constant parameters. The software runs on a computer containing an Intel Core i7-950 3.06 GHz quad-core processor, 24 GB system RAM, a GTX Titan graphics processing unit featuring 2,688 Cuda cores operating at 836 MHz with 6 GB RAM, and that runs on the Linux operating system. The optimizer runtime is on the order of a few tens of minutes, depending on user-defined parameters. The particle swarm optimization seeds a user-defined region of the parameter space with a large number of "particles". The region of the parameter space to be seeded is selected based on expected values of the parameters. For example, the resistance decays from a vertical asymptote as conducted charge increases, and must therefore decay on a very small scale (on the scale of reasonable conducted charge, usually in the µC range). Therefore, only very low values for C_2 and C_4 are seeded in the parameter space. A similar approach is used to determine a seeding range for each

parameter. Each particle represents a unique possible set of constants C_1 - C_{10}, which is represented as a single ten-dimensional point in the parameter space. Each particle is also assigned a "velocity" in the parameter space that determines how far in the parameter space each point may move (equivalently, how much the constants C_1 - C_{10} can change) between iterations of the program. The algorithm updates the velocities of the particles based on the cost value calculated for each point according to Eq. 4.3, and the points' proximity to one another. The goal is to sweep a large range of parameter space with many local minima without having to sweep the whole range with a fine resolution.

The particle swarm optimizer is used to calculate the optimum set of constants for several 3 nF, 2 Ω discharges with various charging voltages. The calculated constants are given in Table 4.1.

The constants exhibit a high degree of variation in order of magnitude due to the nature of the model. The constants function to scale an equation that is base on the current, which may reach values in the kiloampere range, and the total charge conducted, which may reach a maximum as low as a few millicoulomb for larger discharge capacitances charged to the switches maximum voltage rating of 4 kV.

The constants in Table 4.1, in conjunction with Eq. 4.2, define a surface, which is plotted in Fig. 4.6, with reasonable agreement with the observed resistance waveforms.

Table 4.1: Optimized constant parameter values for 3 nF discharging into 2 Ω.

Constant Parameter	Optimized Value
C_1	3.399×10^{-3}
C_2	2.536×10^{-1}
C_3	1.488×10^{-2}
C_4	4.712×10^{-1}
C_5	3.605×10^{-5}
C_6	2.037×10^{-4}
C_7	2.154
C_8	7.075×10^{-7}
C_9	9.747×10^{-6}
C_{10}	4.000×10^{-4}

4.2 High Current Considerations

The model thus presented is reasonable for over damped, low current discharges that do not involve high di/dt. For the model to be useful in high-current pulse generator development, however, certain considerations must be taken that are unaddressed by the model described by Eq. 4.2.

For discharges involving a large capacitance and low load resistance, the total charge that passes through the switch may be in the millicoulomb range. It can be seen by inspection of Eq. 4.2 that as the total conducted charge $\int I dt$ increases, the

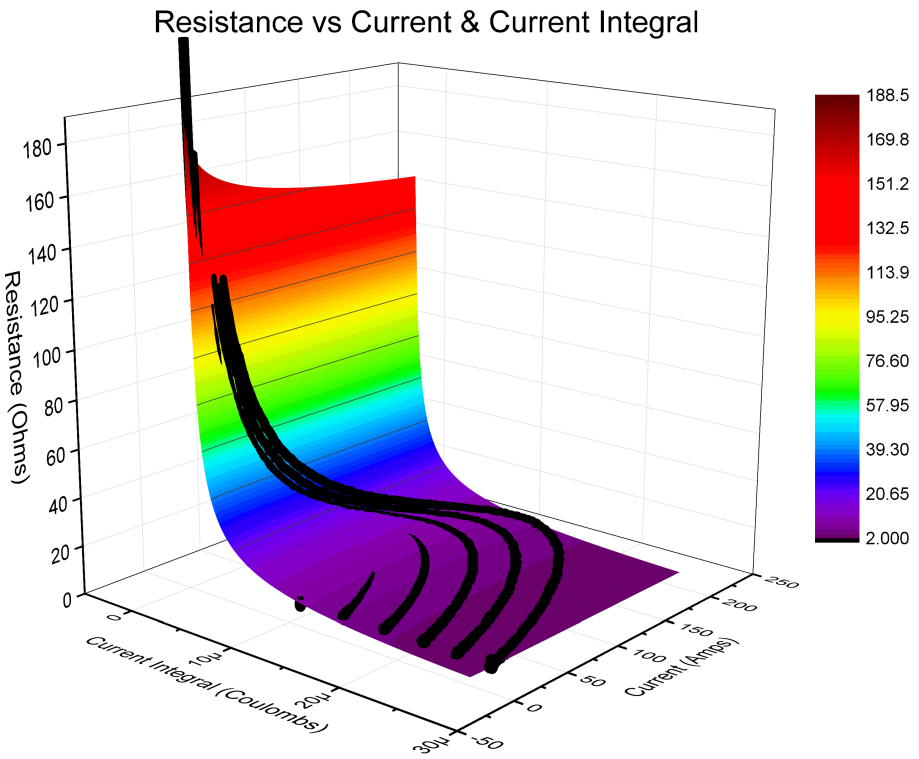

Figure 4.6: Equivalent switch resistance vs instantaneous current and total charge conducted model/experiment comparison for constants given in Table 4.1.

modeled equivalent switch resistance approaches zero. In simulation, this may result in high-Q oscillations that are not observed in experiments.

Additionally, if the circuit being simulated has a low series inductance, the current through the switch may increase quickly. The CCS-SC-14N40 has a maximum rate of current increase rating of 30 kA/µs. In such cases the inductance in the switch packaging may be large enough to affect the performance of the device.

Fig. 4.7 shows typical voltage vs time and current vs time waveforms for a high current discharge.

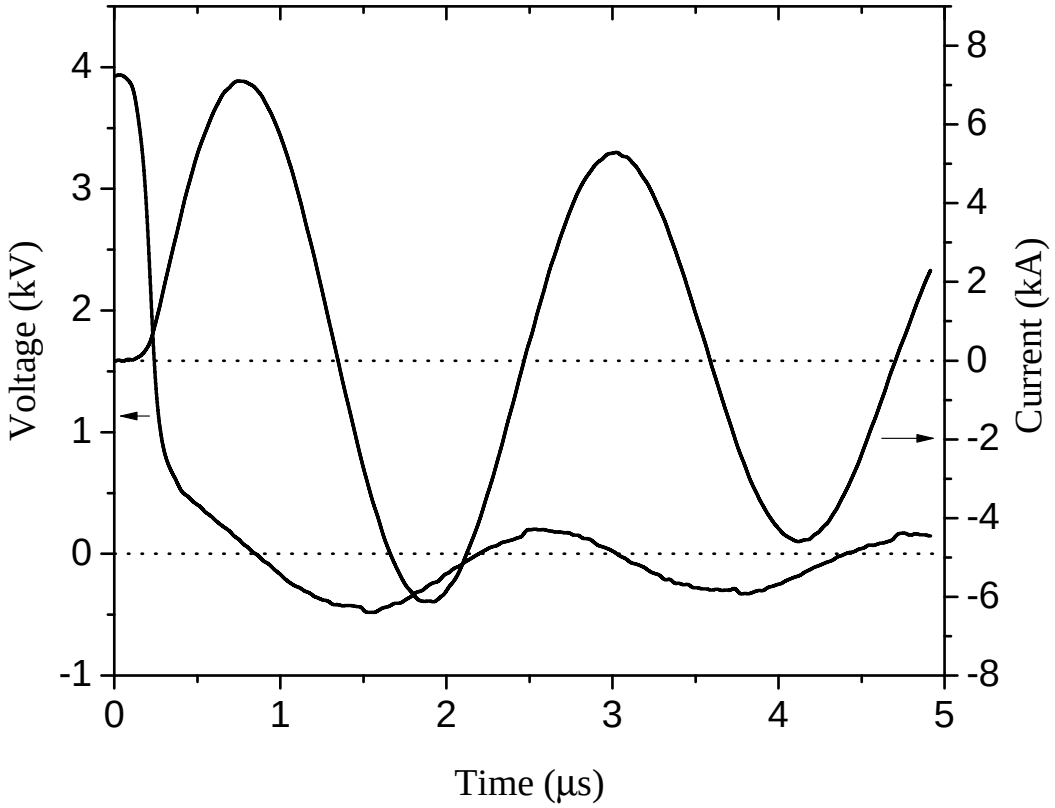

Figure 4.7: Voltage and current vs time waveforms for 660 nF charged to 4 kV, discharged into a shorted load. Arrows indicate axis association.

4.2.1 On-State Resistance

It is noted that the current vs time waveforms observed in Fig. 4.7 is an exponentially decaying sinusoid. This indicates that once the thyristor has turned on, the device can be described as an on-state resistance. Similarly to the transient resistance given by Eq. 4.2, it is likely that the on-state resistance may be related to the current passing through the device.

Measurement of the thyristor's on-state resistance is accomplished by observing the decay and fundamental frequency of the oscillating current waveform, with the assumption that losses in the conductors between circuit elements are negligible. For

an underdamped series RLC circuit, Eq. 4.4 gives the series resistance in terms of the exponential decay constant α and the total series inductance L_{tot}. The full solution to the series R-L-C circuit is given in Appendix A.

$$R_{series} = 2\alpha L_{tot} \tag{4.4}$$

To calculate the series resistance in the circuit, the exponential decay constant α and the total series inductance L_{tot} must be calculated.

The total series inductance is expressed in Eq. 4.5 in terms of the discharge capacitance C and the resonant frequency f_r.

$$L_{tot} = \frac{1}{4\pi^2 f_r^2 C} \tag{4.5}$$

The discharge capacitance C is known, so only the resonant frequency f_r must be determined. Because the time-average of the current waveform is positive, a discrete Fourier Transform of the current waveform results in a DC component that overwhelms the resonant frequency. To eliminate the DC bias, a discrete Fourier transform is taken of the time-derivative of the current waveform.

The digitization error, noise, and high sampling rate of the oscilloscope make differentiation of the raw current waveform futile. Before the waveform can be differentiated, a 20,000-order digital low-pass filter with a cut-off frequency of 7 MHz is implemented using MATLAB's digital signal processing capabilities. Fig. 4.8 shows the difference between the current waveform before and after filtering.

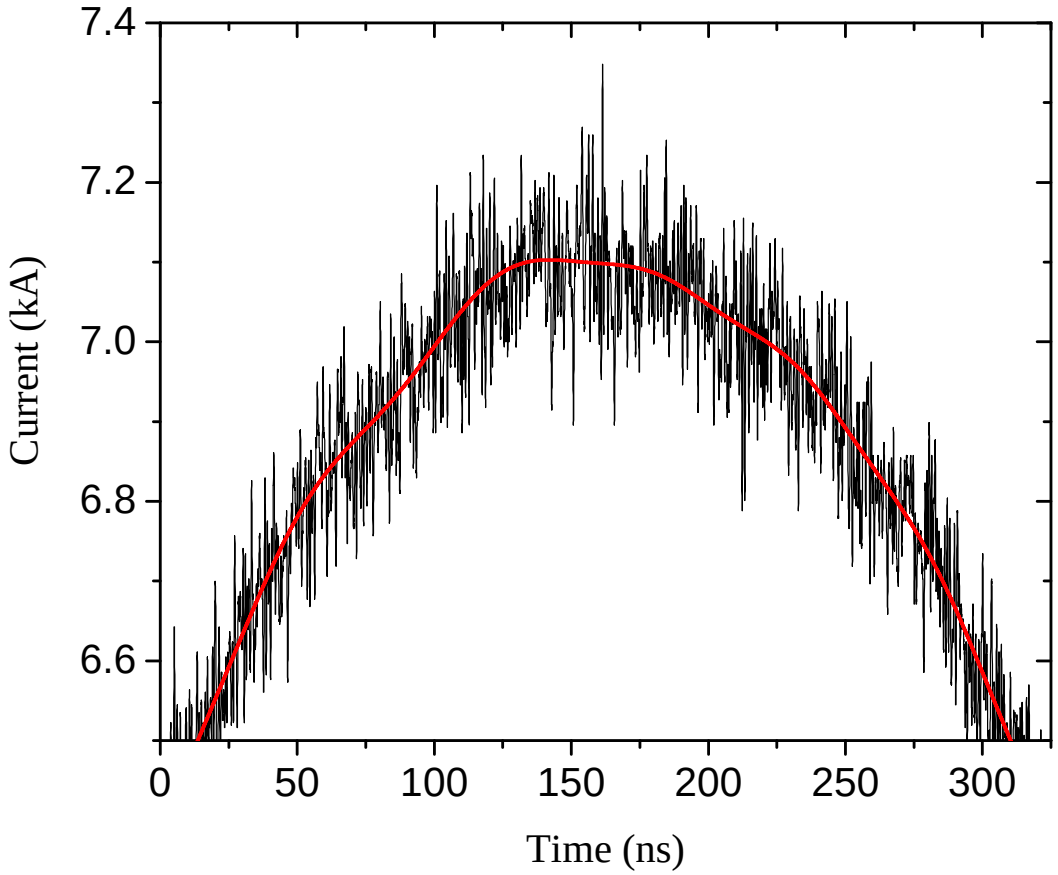

Figure 4.8: Comparison waveform for filtered and unfiltered current vs time data.

It is seen in Fig. 4.8 that the time-derivative of the unfiltered waveform would be dominated by noise, and would not accurately reflect the actual di/dt of the discharge.

After filtering, the time-derivative of the waveform is estimated via central difference approximation. Fig. 4.9 shows the derivative of the current waveform shown in Fig. 4.7.

After differentiation, the discrete Fourier transform is taken in order to observe the fundamental frequency. Fig. 4.10 shows the frequency content of the di/dt waveform shown in Fig. 4.9.

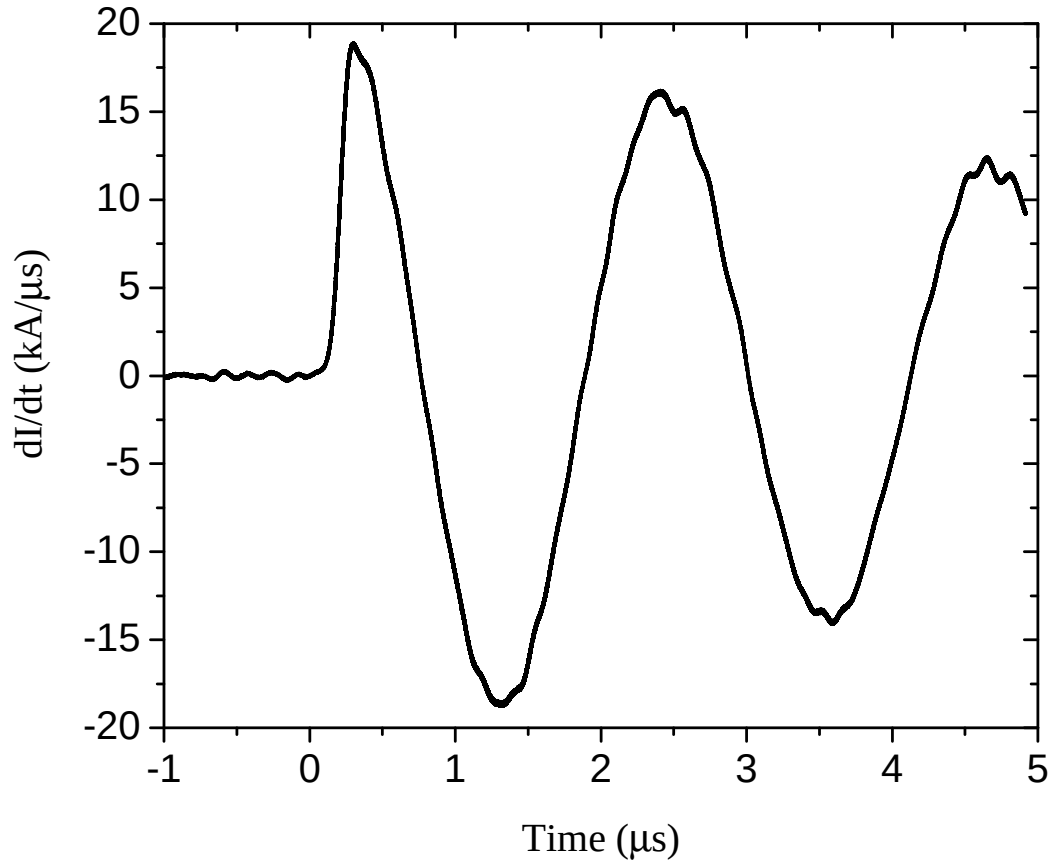

Figure 4.9: Time-derivative of the current waveform shown in Fig. 4.7.

The resonant frequency f_r is readily observed in Fig. 4.10, and together with the discharge capacitance C, yields the total series inductance according to Eq. 4.5.

The decay constant α is calculated by observing the first two local maxima in the current waveform, $I_{max,1}$ and $I_{max,2}$, and the times at which those maxima occur, t_1 and t_2, respectively. The decay constant is then calculated using Eq. 4.6.

$$\alpha = \frac{\ln\left(I_{max,1}/I_{max,2}\right)}{t_2 - t_1} \tag{4.6}$$

The decay constant α, calculated from Eq. 4.6, and the total series inductance L_{tot}, calculated from Eq. 4.5, yield the total series resistance given in Eq. 4.4. The

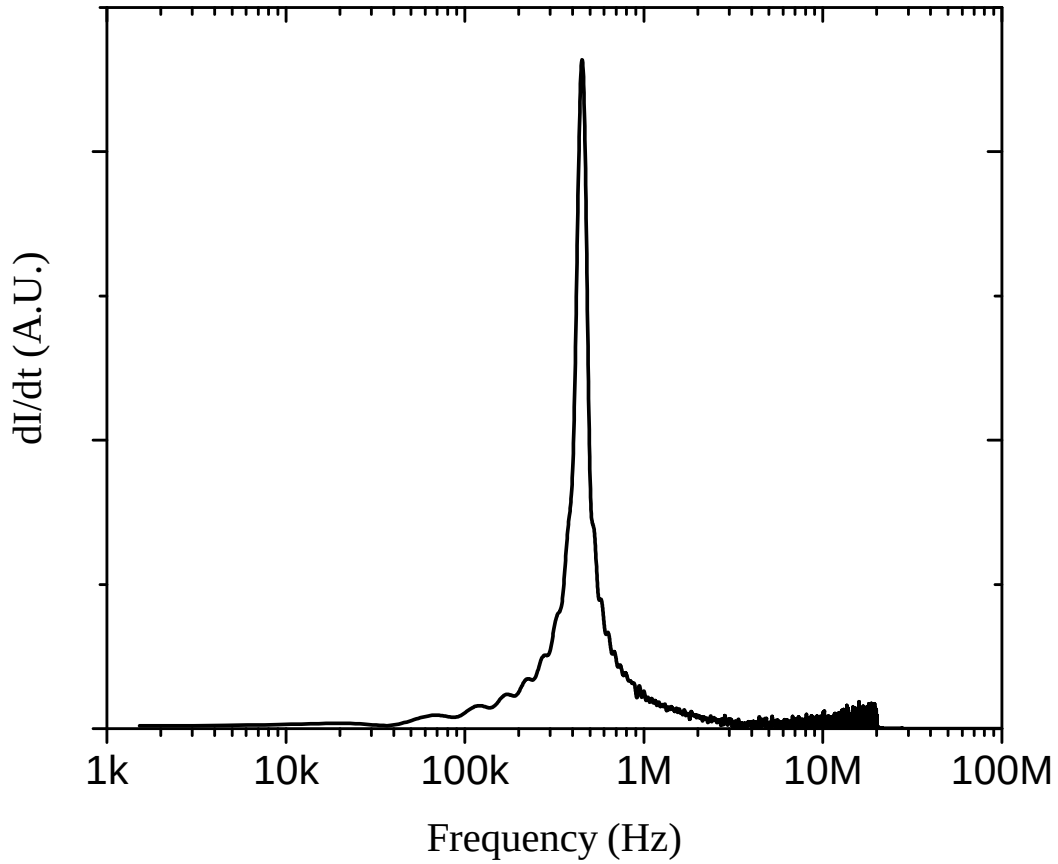

Figure 4.10: Frequency content of the di/dt waveform shown in Fig. 4.9.

resistance in the conductors that connect circuit element is considered to be negligible. The capacitor bank series resistance is given as a dissipation factor, which is a function of frequency, in the manufacturer's data sheet [18]. The dissipation factor is extrapolated from given data points, and the ESR (capacitor estimated series resistance) is calculated using Eq. 4.7.

$$ESR = \frac{DF}{2\pi f_r C} \tag{4.7}$$

The capacitor ESR is found to be on the order of 10 mΩ, which is significantly less than the calculated total series resistances. The capacitor ESR is subtracted from

the total series resistance, and the difference is taken to be the on-state resistance of the thyristor, as given in Eq. 4.8.

$$R_{on,thy} = R_{series} - ESR \tag{4.8}$$

Because measurement of the on-state resistance of the switch requires an underdamped circuit, data for evaluation of the on-state resistance is always taken with a shorted load. The discharge capacitance and charging voltages are varied. The measured on-state resistance of the switch $R_{on,thy}$ is plotted vs the peak current I_{peak} in Fig. 4.11.

The inversely proportional fit given by Eq. 4.9 is applied and also shown in Fig. 4.11.

$$R_{on,thy}(I_{peak}) = aI_{peak}^{-b} + d \tag{4.9}$$

Here, a, b, and d are model parameters used to fit the model to experimental data.

This model is optimized via gradient descent minimization of the cost function given by Eq. 4.10.

$$Err = \sum_{n=1}^{N} \frac{|R_{on,thy}(I_{peak}) - R_n|}{N} \tag{4.10}$$

Optimization yields $a = 127.8$, $b = 1.043$, and $d = 0.02143$. The on-state resistance given by Eq. 4.9 is added to the expression given in Eq. 4.2 to give the total switch resistance for high-current discharges.

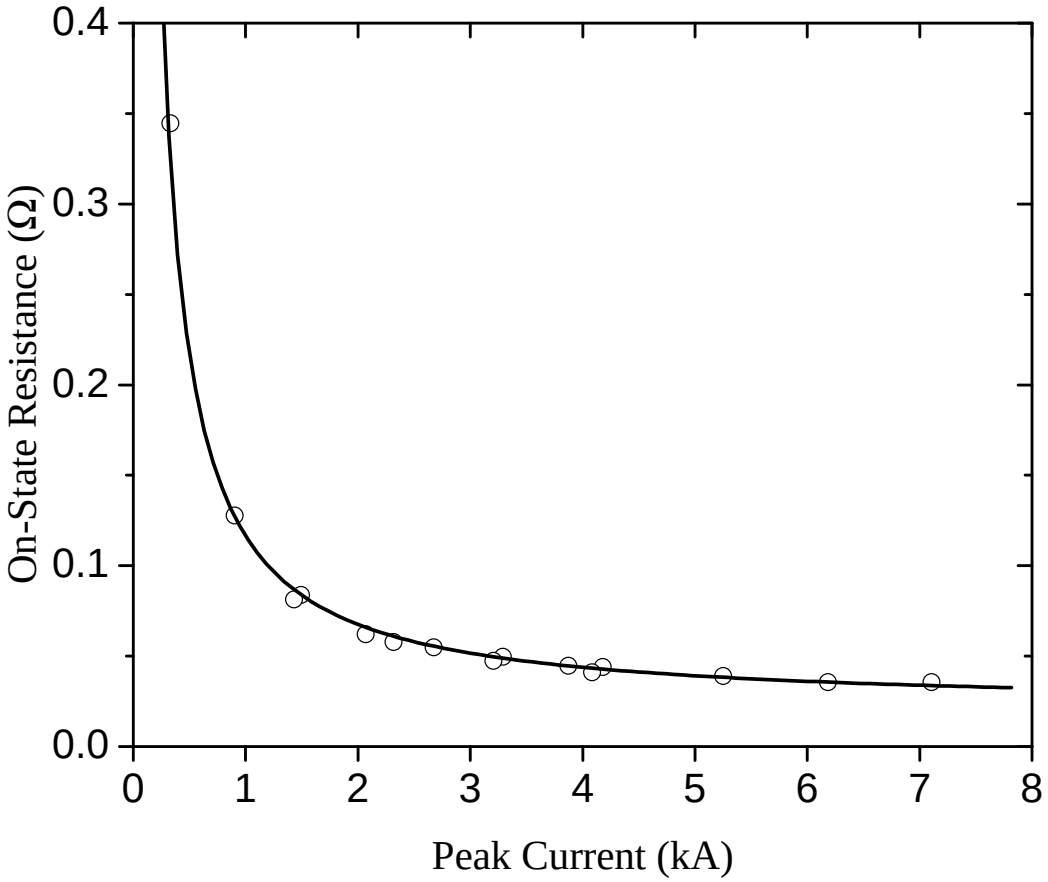

Figure 4.11: On-state thyristor equivalent resistance vs peak current, with empirical fit given by Eq. 4.9. Discharges varied capacitance and charging voltage into a shorted load.

$$R_{thy,highI} = R_{thy} + R_{on,thy} \tag{4.11}$$

4.2.2 Switch Internal Inductance

A lumped inductance L_{thy} is added to the model to account for high di/dt effects. The internal switch inductance is measured by observing the voltage and current waveforms for a 660 nF capacitor charged to 4 kV, discharged into a shorted load, as shown in Fig. 4.7.

The experimentally measured voltage waveform can be modified to isolate the portion of the voltage that is due purely to the switch's on-state resistance by subtracting the inductive voltage drop, shown in Eq. 4.12.

$$V_{thy,mod} = V_{thy,meas} - L_{est}\frac{di}{dt} \tag{4.12}$$

Here, $V_{thy,mod}$ represents the modified voltage waveform that reflects only the voltage associated the the switch resistance. $V_{thy,meas}$ refers to the experimentally measured voltage waveform. L_{est} represents the estimated switch inductance, and di/dt represents the time-derivative of the current waveform, as shown in Fig. 4.9.

The discrete Fourier transform of the modified voltage waveform $V_{thy,mod}(t)$ and of the current waveform is evaluated only at the resonant frequency using Eq. 4.13.

$$\mathcal{F}\{x(t)\}(f = f_r) = \sum_{n=2}^{N} \frac{1}{2}(x_n e^{-j2\pi f_r t_n} + x_{n-1} e^{-j2\pi f_r t_{n-1}})(t_n - t_{n-1}) \tag{4.13}$$

Here, x_n represents the n^{th} data point to be recorded by the oscilloscope in either the voltage or the current waveform. t_n represents the time at which x_n is observed. N represents the total number of data points begin considered, and f_r represents the resonant frequency.

To prevent the transient turn-on portion of the waveforms from affecting the Fourier transform, only data points that occur after the first zero-crossing of the voltage waveform are considered.

The Fourier transform at the resonant frequency gives a complex number X_{f_r} with a real and imaginary portion. The phase angle θ_{f_r} is of interest here, and is obtained from the real and imaginary parts of X_{f_r} by Eq. B.6.

$$\theta_{f_r} = \sin^{-1}\left(\frac{\Im\{X_{f_r}\}}{\Re\{X_{f_r}\}}\right) \tag{4.14}$$

The phase difference $\Delta\theta_{f_r}$ between current and voltage waveforms is given in Eq. 4.15.

$$\Delta\theta_{f_r} = \theta_{I,f_r} - \theta_{V,f_r} \tag{4.15}$$

The phase difference $\Delta\theta_{f_r}$ between the current waveform and the modified voltage waveform (given in Eq. 4.12) at the resonant frequency is plotted against the estimated switch inductance L_{est} in Fig. 4.12.

According to circuit theory, when the correct switch inductance is chosen, the phase difference between the current and the modified voltage waveforms is zero. Therefore, the switch inductance is taken to be the inductance that produces zero phase difference in Eq. 4.15 and Fig. 4.12. The internal switch inductance is found to be 16.6 nH.

4.3 Model Implementation

The presented model is implemented for used in LTSPICE circuit simulation software. Fig. 4.13 shows the schematic of the SPICE sub-circuit.

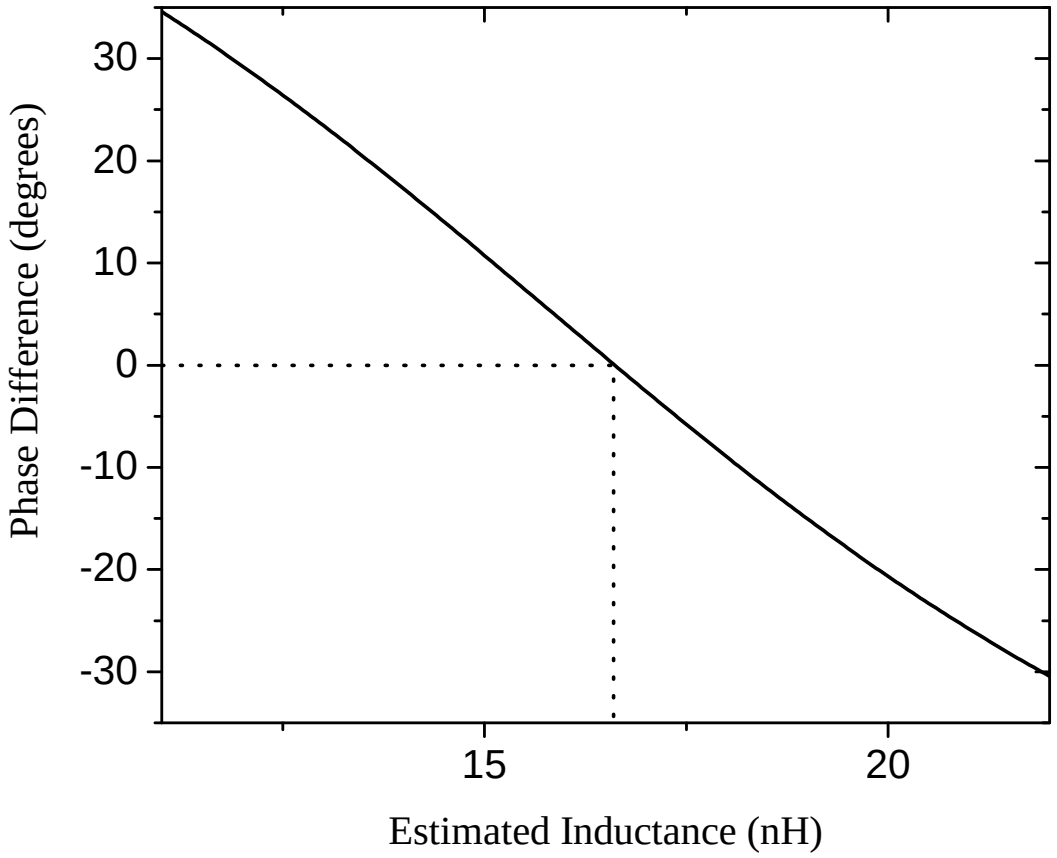

Figure 4.12: Phase difference between current and modified voltage waveforms at the resonant frequency vs estimated switch inductance. Drop lines indicate zero crossing.

The variable resistance is realized in the SPICE sub-circuit as a behavioral current source that drives a current equal to the ratio of the voltage drop across the switch terminal nodes (nodes "A" and "K") to the calculated equivalent resistance value, as given in Eq. 4.16.

$$I_{thy,source} = \frac{V_{AK}}{R_{thy}\left(I, \int I dt\right)} \tag{4.16}$$

To avoid unintentional triggering due to numerical errors or the slow build-up of conducted charge that would eventually occur even if the resistance were extremely

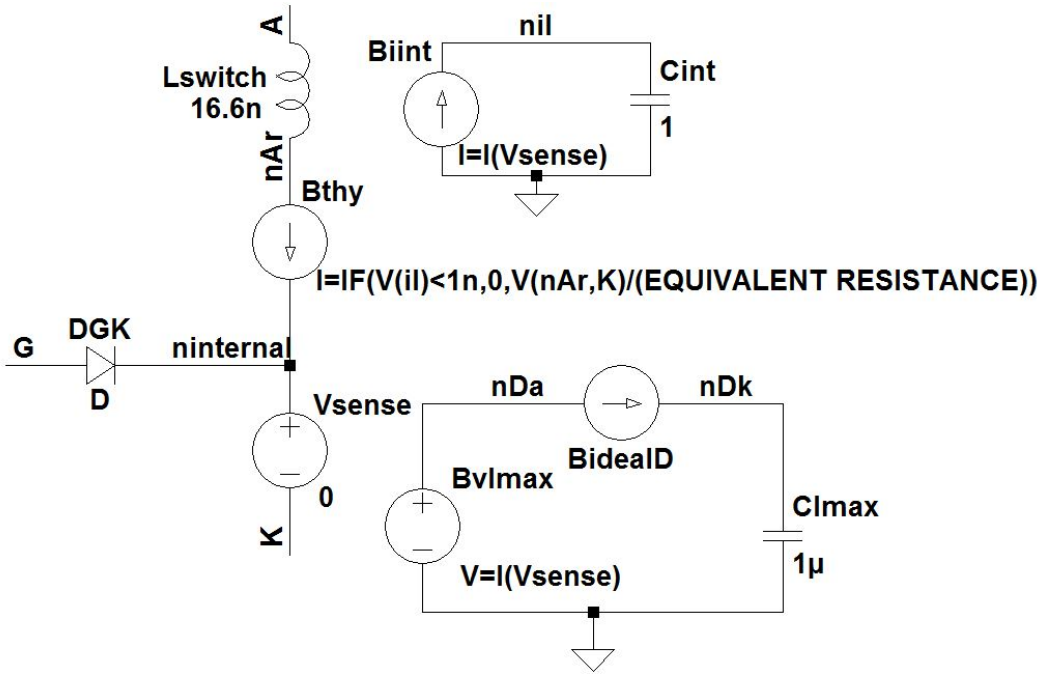

Figure 4.13: Circuit schematic for the SPICE sub-circuit implementation of the thyristor model.

high, the behavioral current source is modified with an IF statement so that zero current is sourced until at least 1 nC has passed through the cathode of the device.

Measurement of the instantaneous current is accomplished using the voltage source "Vsense". Because SPICE programs keep track of the current through voltage sources during runtime, a 0 V ideal source is the ideal method for measuring current to adjust device behavior.

The device is triggered by driving a current into node "G" and out of node "K". "Vsense" is placed so that this current will contribute to the total conducted charge, and result in a finite equivalent switch resistance.

The total charge conducted is measured by using a behavioral current source, "Biint", to drive a current equal to the cathode current into a 1 F capacitor, "Cint". From circuit theory, the voltage across the capacitor is given in by Eq. 4.17.

$$v_C(t) = \frac{1}{C}\int_0^t i(\tau)d\tau + V_0 \tag{4.17}$$

Here, τ is a replacement variable for time. After the integration is carried out, the resulting expression is a function of t. V_0 refers to the voltage across the capacitor at time $t = 0$, which is set to 0 V.

Because "Cint" has a value of 1 F, the expression given in Eq. 4.17 resolves to a value equal to the total charge that has passed through the device, as shown in Eq. 4.18, with the only difference being the units.

$$v_C(t) = \frac{1}{C = 1}\int_0^t i(\tau)d\tau + (V_0 = 0) = C(t) \tag{4.18}$$

The voltage at node "niI" is then substituted for $\int Idt$ in Eq. 4.2.

For calculation of the on-state resistance, the peak current I_{peak} is measured by using a behavioral voltage source, "BvImax", to supply a voltage equal to the instantaneous current in the device. A behavioral current source "BidealD" is used to act as an ideal diode. "BidealD" acts as a resistance supplying a current proportional to the voltage across it divided by the value of the resistance. When the voltage drop from node "nDa" to node "nDk" is positive, the equivalent resistance of "BidealD" is 1 nΩ. When the voltage drop from node "nDa" to node "nDk" is negative, the

equivalent resistance of "BidealD" is 1 GΩ. The voltage at node "nDk" is then equal to the peak current, and is substituted for I_{peak} in Eq. 4.9.

A SPICE model diode is placed between nodes "G" and the internal node "ninternal" to approximate the behavior of the *pn* junction between the gate and cathode terminals during gating.

The switch inductance L_{thy} is included in the switch model as the lumped element inductor "Lswitch", and is given the measured value of 16.6 nH.

Because SPICE is a hardware description language, the circuit shown in Fig. 4.13 is implemented as a SPICE sub-circuit, which is described by the netlist code in Fig. 4.14.

```
*  Thyristor
*                A G K
.subckt Thyristor A G K
DGK G ninternal1 D
Lthy A ninternal2 16.6n
Bthy ninternal2 ninternal1 I=IF(V(niI)<1n,0,V(ninternal2,K)/(EQUIVALENT RESISTANCE))
Vsense ninternal1 K 0
Bint 0 niI I=I(Vsense)
Cint 0 niI 1
Bmax1 nDa 0 V=I(Vsense)
Bmax2 nDa nDk I=IF(V(nDa,nDk)>0,V(nDa,nDk)/1e-9,V(nDa,nDk)/1e9)
Cmax 0 nDk 1u
.ic V(niI)=0
.ic V(nDk)=0
.model D D
.end Thyristor
```

Figure 4.14: SPICE sub-circuit netlist implementation of the circuit in Fig. 4.13.

Additionally, an LTSPICE schematic symbol, shown in Fig. 4.15, is designed to represent the device in simulation schematics.

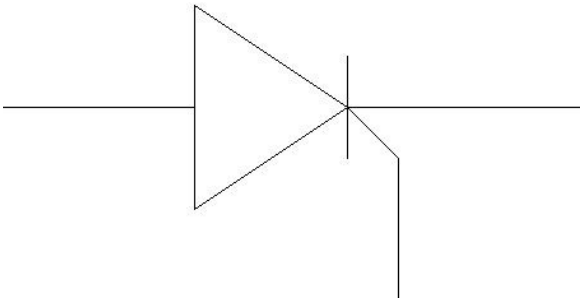

Figure 4.15: LTSPICE schematic symbol for the sub-circuit netlist shown in Fig 4.14.

4.4 Model/Experiment Comparison

The model is validated by comparison to experimental waveforms obtained from discharging various capacitances into various loads. The simulated circuit is shown in Fig. 4.16.

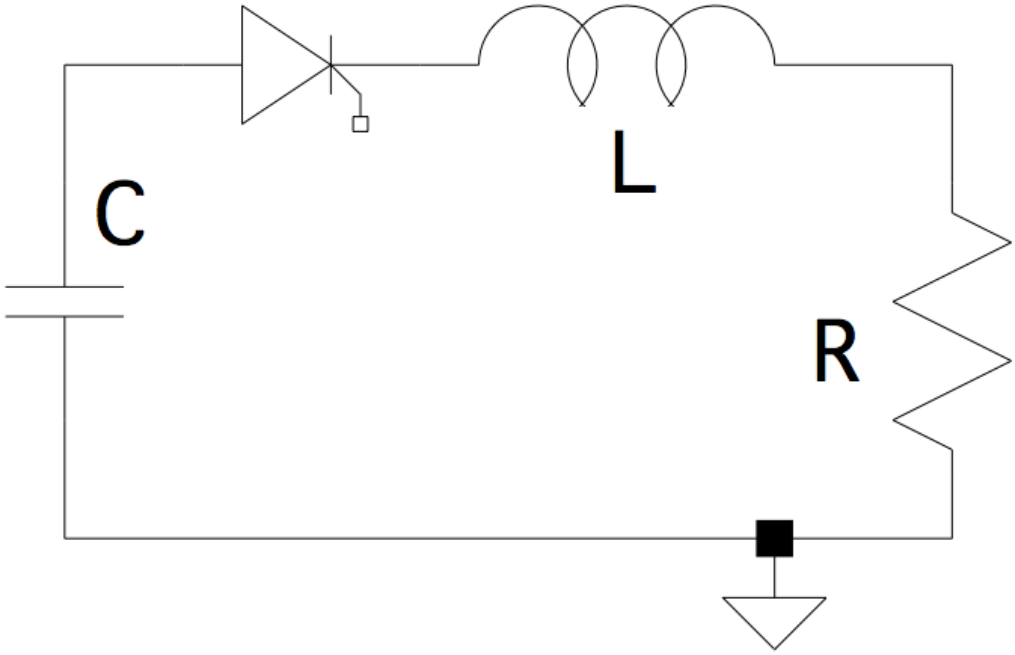

Figure 4.16: Circuit simulated in LTSPICE to generate waveforms for model/experiment comparison.

Simulated waveforms are compared to experimental waveforms with reasonable agreement. Fig. 4.17 compares waveforms for a low-current discharge, Fig. 4.18 compares waveforms for a higher-current discharge, and Fig. 4.19 compares waveforms for a discharge near the current limitation of the device.

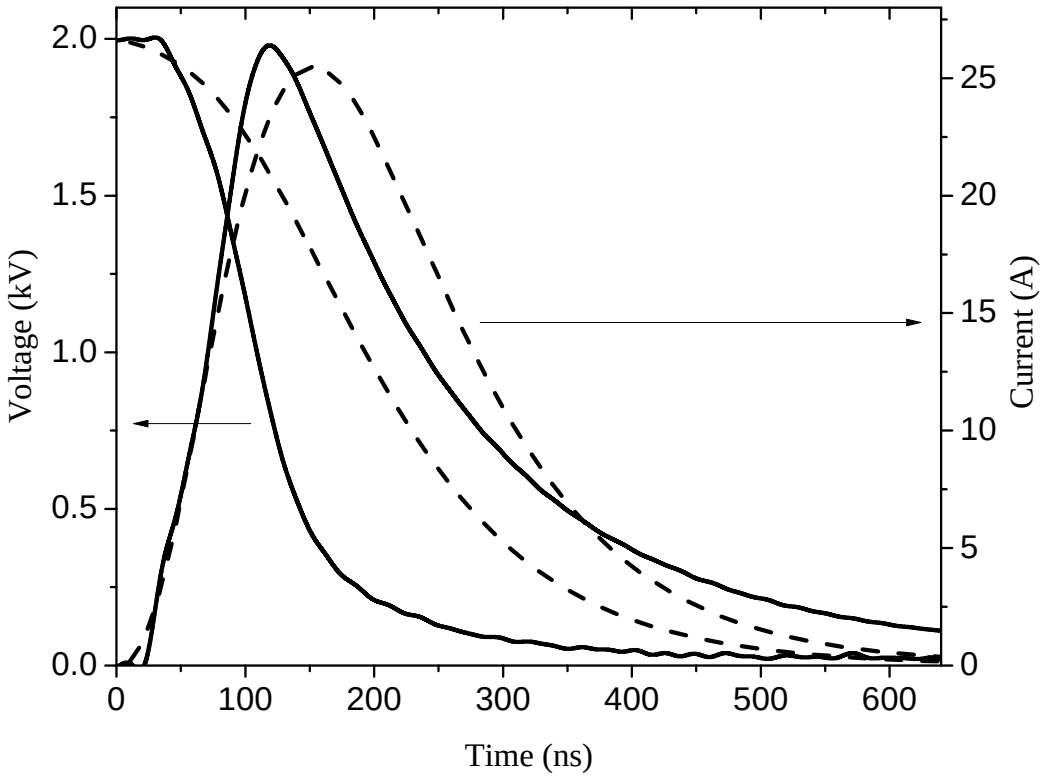

Figure 4.17: Model/experiment comparison voltage and current vs time waveforms for 3 nF charged to 2 kV discharged into 20 Ω. Solid line - measured waveforms, dashed line - simulated waveforms. Arrows indicate axis association.

The compared waveforms shown in Fig. 4.17 display reasonable agreement. The 10% - 90% current rise time in the experiment is 69 ns, and the simulated rise time is 87 ns. This yields an absolute error of 18 ns and a relative error of 26%.

The peak measured current in the experiment is 26.4 A, and the simulated peak current is 25.5 A, yielding an absolute error of 0.9 A and a relative error of 3.4%.

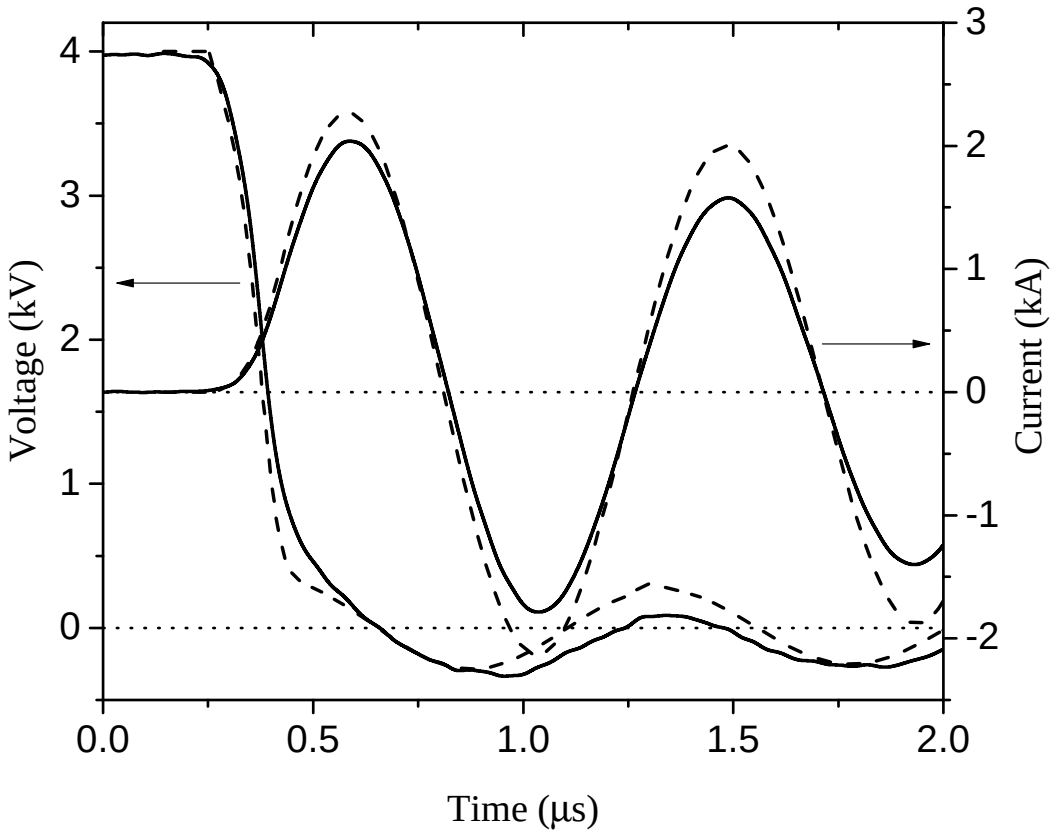

Figure 4.18: Model/experiment comparison voltage and current vs time waveforms for 89 nF charged to 4 kV discharged into a shorted load. Solid line - measured waveforms, dashed line - simulated waveforms. Arrows indicate axis association.

The compared waveforms shown in Fig. 4.18 also display reasonable agreement. Because the current rise time is significantly influenced by stray inductance in the circuit, and because the circuit exhibits damped oscillations, additional calculations are carried out to quantify the model's performance.

The current rise time in the experiment is measured to be 188 ns, and the simulated current rise time is 172 ns, giving an absolute error of 16 ns and a relative error of 8.6%.

Because the pulse rise time is significantly affected by stray inductance, the di/dt rise time may also be a useful quantity of comparison. In the experiment, the di/dt rise time is measured to be 102 ns, and the simulated di/dt rise time is 143 ns, yielding an absolute error of 42 ns and a relative error of 41%.

The peak current in the experiment is measured to be 2.09 kA, and the simulated peak current is 2.27 kA, yielding an absolute error of 180 A and a relative error of 8.9%.

The on-state resistance of the switch in the experiment is measured to be 128 mΩ, and the simulated on-state switch resistance is 61 mΩ, yielding an absolute error of 67 mΩ and a relative error of 52.6%.

The phase difference between the oscillating current and voltage waveforms in the experiment is measured to be 33°, and the phase difference between the voltage and current waveforms in simulation is 64°, yielding an absolute error of 31°, or 8.6% of one cycle.

The comparison waveforms in Fig. 4.19 show excellent agreement. The same quantities of comparison used to characterize the model's performance in Fig. 4.18 are calculated for Fig. 4.19 with relative errors below 5% for all quantities.

The current rise time in the experiment is measured to be 385 ns, and the simulated current rise time is 371 ns, giving an absolute error of 14 ns and a relative error of 3.6%.

In the experiment, the di/dt rise time is measured to be 116 ns, and the simulated di/dt rise time is 119 ns, yielding an absolute error of 3 ns and a relative error of 2.9%.

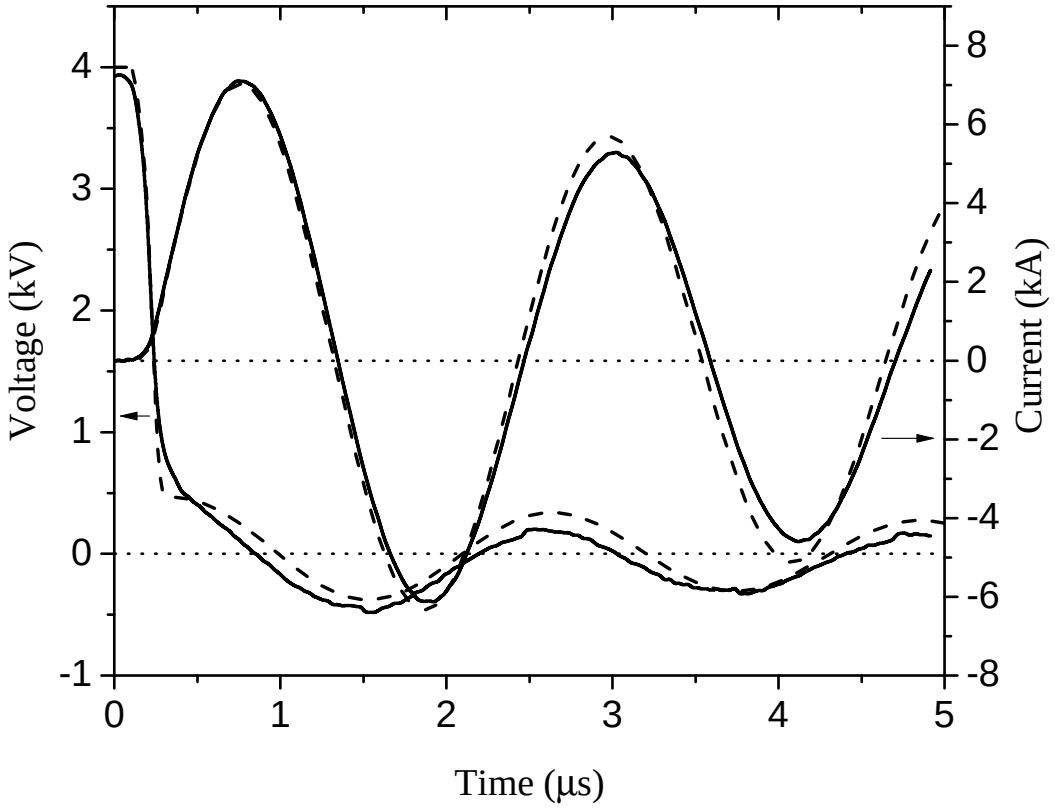

Figure 4.19: Model/experiment comparison voltage and current vs time waveforms for 660 nF charged to 4 kV discharged into a shorted load. Solid line - measured waveforms, dashed line - simulated waveforms. Arrows indicate axis association.

The peak current in the experiment is measured to be 7.11 kA, and the simulated peak current is 6.92 kA, yielding an absolute error of 190 A and a relative error of 2.7%.

The on-state resistance of the switch in the experiment is measured to be 33.7 mΩ, and the simulated on-state switch resistance is 34.3 mΩ, yielding an absolute error of 0.6 mΩ and a relative error of 1.8%.

The phase difference between the oscillating current and voltage waveforms in the experiment is measured to be 57°, and the phase difference between the voltage and

current waveforms in simulation is 40°, yielding an absolute error of 17°, or 4.7% of one cycle.

It is noted that the model's accuracy is improved for high current discharges. This phenomenon is a result of the tendency for high current discharges to be dominated by the thyristor's on-state resistance and internal switch inductance. Modeling these two switch characteristics is trivial compared to the highly non-linear behavior of the switch as it transitions from off to on, which tends to dominate low current discharges.

All compared waveforms show reasonable agreement, indicating that the model is useful for approximating the performance of the switch in a pulsed power generator simulation.

CHAPTER 5

FUTURE WORK

The thyristor SPICE model is intended for use in the design and simulation of a solid-state pulse generator. A linear transformer driver [7, 8] topology is selected for it's modular distribution of stress. The circuit schematic for a linear transformer driver is shown in Fig. 5.1.

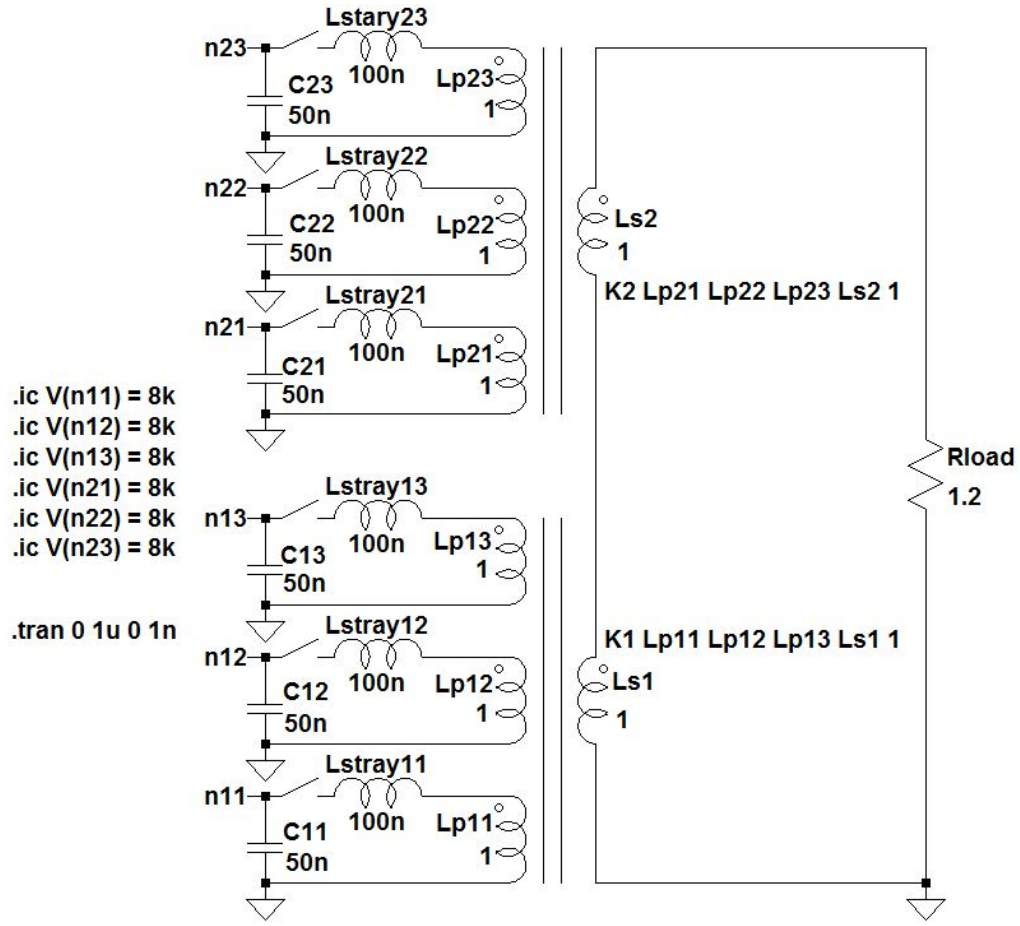

Figure 5.1: 2-stage linear transformer driver (LTD) circuit schematic with 3 bricks per stage and ideal switches.

The circuit shown in Fig. 5.1 features 2 stages with 3 bricks per stage. Stray inductance is included to highlight the LTD feature of primary inductance division. Discharging the capacitors through multiple switches around a single core allows for significant division and reduction of the inductance in the primary winding. The geometry of the device can be designed to minimize inductance in the secondary winding, allowing for very low inductance pulse generators suited for driving low-impedance loads.

In addition to primary inductance division, the LTD design features inductive voltage addition, so that the output pulse voltage is equal to the product of the charging voltage and the number of stages, neglecting parasitics. All stages are charged with reference to a common ground potential.

Fig. 5.2 shows the voltage across a single primary winding and the voltage across the secondary winding vs time for the circuit shown in Fig. 5.1, and Fig. 5.3 shows the current through a single switch and the current in the secondary winding vs time.

The switch model presented will be used to design and analyze possible circuit configurations for a solid-state LTD utilizing the CCS-SC-14N40 thyristor-type switch.

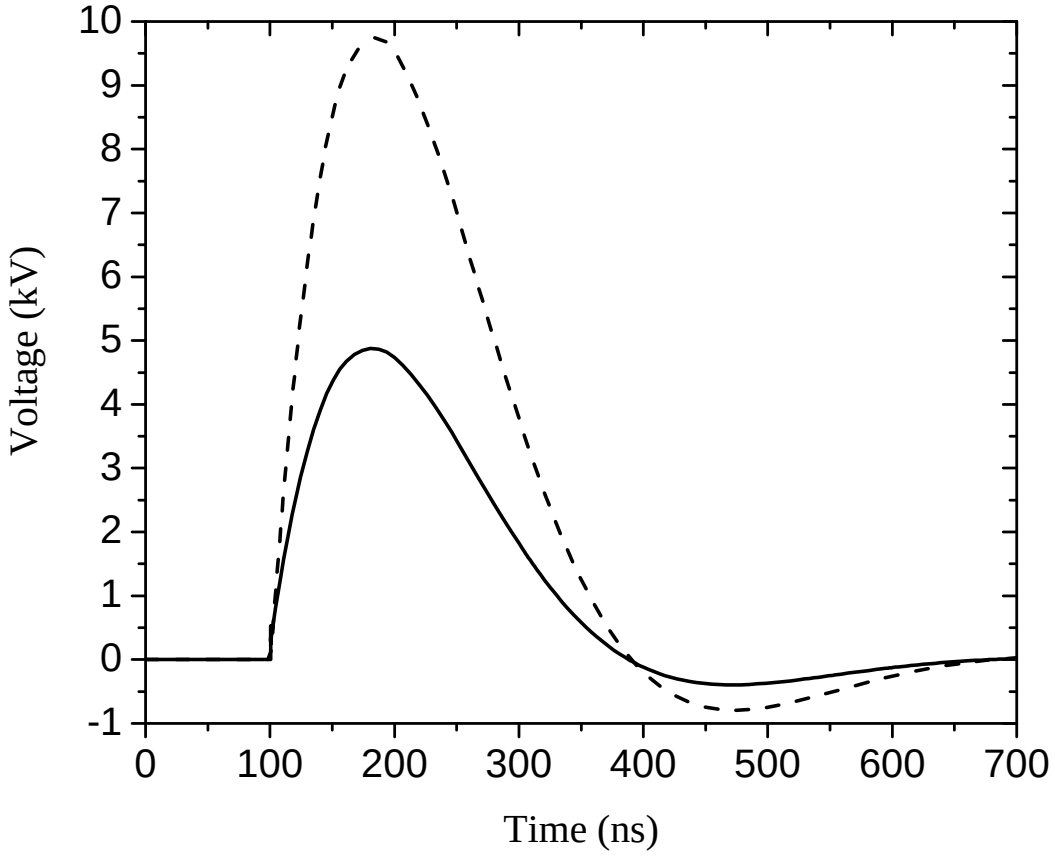

Figure 5.2: Primary and secondary winding voltage vs time comparison waveforms for an ideal 2-stage LTD with 3 bricks per stage.

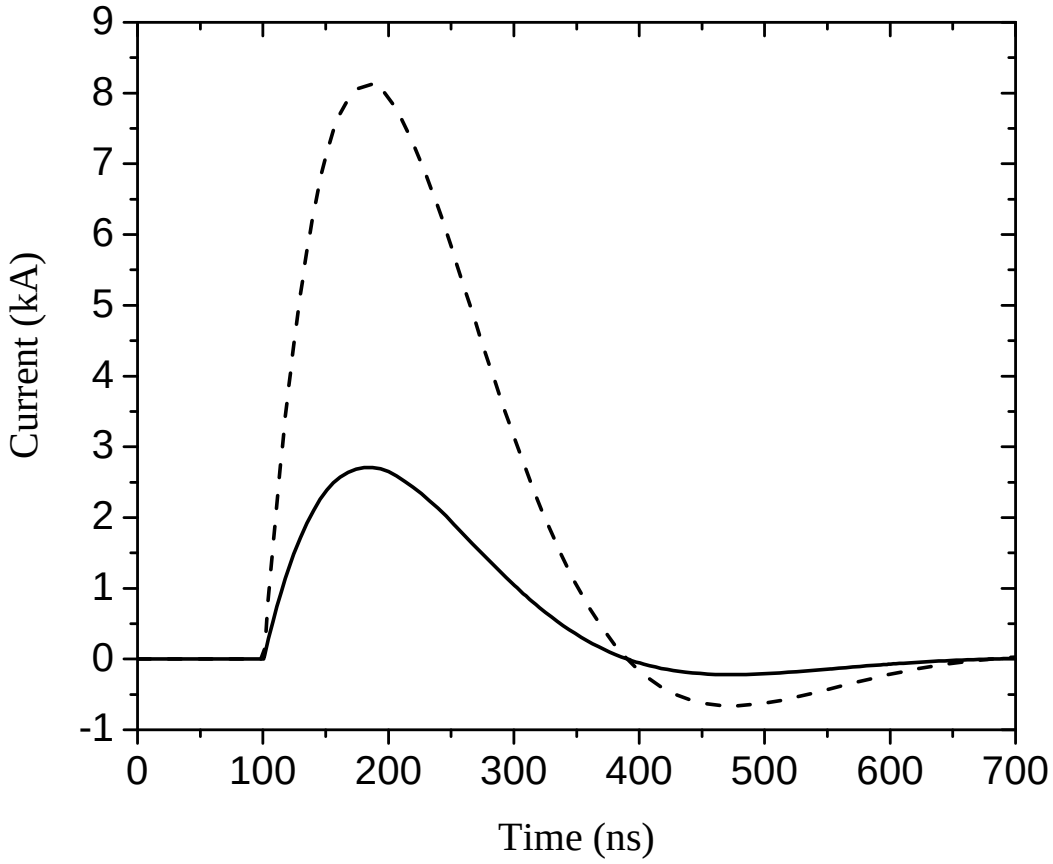

Figure 5.3: Single brick current and secondary winding current vs time comparison waveforms for an ideal 2-stage LTD with 3 bricks per stage.

CHAPTER 6

CONCLUSION

An empirical technique for modeling the transient behavior of thyristor-type switches is presented. The process of model determination is detailed for Silicon Power's CSS-SC-14N40 thyristor-type switch. The model is implemented as a SPICE sub circuit, and LTSPICE is used to simulate various R-L-C discharges. The simulated voltage and current vs time waveforms are compared to experimental waveforms with reasonable agreement.

The model is intended to be used in the development and design of a solid-state linear transformer driver (LTD) high power pulse generator. The LTD generator is indented to replace an existing gas-switched PFN-based Marx generator which is currently being used to drive high power loads such as a virtual cathode oscillator (vircator) high power microwave device. A solid state LTD generator may prove to be superior to a gas-switched Marx generator in lifetime, reliability, size, jitter, and required charging voltage.

REFERENCES

[1] Silicon Power, "CCS-SC-14N40 Datasheet," siliconpower.com., July 2008.

[2] L. Giacoletto, "Simple SCR and TRIAC PSPICE Computer Models," *IEEE Transactions on Industrial Electronics.*, Vol. 36, No. 3, pp. 451-455, August 1989.

[3] G. Sayah, A. Zekry, H. Ragaie, F. Soliman, "A SPICE Model of a Thyristor with High Injection Effects and Conductivity Modulation," *Proc. of the 15th International Conference on Microelectronics (ICM).*, pp. 344-347, 2003.

[4] A. Shaker, G. Sayah, M. Agouelatta, A. Zekry, "Thyristor Compact Modeling based on Gummel-Poon Model Including Parameter Extraction Procedure," *International Journal of Computer Applications.*, Vol. 61, No. 16, pp. 10-12, January 2013.

[5] H. D. Sanders, S. C. Glidden, "High Current, High di/dt, Solid State Switch Resistance Model," *Proc. of the 2008 International Power Modulators and High Voltage Conference*, pp. 366-368, May 27-31, 2008.

[6] J. Parson, B. Bragg, M. Tayor, D. Barnett, "Rep-Rate Operation of a 200 kV Sealed-Tube Reflex-Triode Vircator at 200A/cm^2," *Proc. of the International Conference on Plasma Science*, 2014.

[7] W. Jiang, "Solid-State LTD Module Using Power MOSFETs," *IEEE Transactions On Plasma Science*, Vol. 38, No. 10, pp. 2730-2733, October 2010.

[8] W. Jiang, H. Sugiyama, A. Tokuchi, "Pulsed Power Generation by Solid-State LTD," *IEEE Transactions on Plasma Science*, Vol. 42, No. 11, pp. 3603-3608, November 2014.

[9] S. T. Thornton, A. Rex, *Modern Physics for Scientists and Engineers*, Saunders College Publishing, Wadsworth, 1993.

[10] E. Nasser, *Fundamentals of Gaseous Ionization and Plasma Electronics*, Wiley Series in Plasma Physics, Wiley-Interscience, New York, 1971.

[11] A. S. Sedra and K. C. Smith, *Microelectronic Circuits*, Oxford University Press, Oxford, New York, 2004.

[12] W. F. Brinkman, D. E. Haggan, W. W. Troutman, "A History of the Invention of the Transistor and Where It Will Lead Us," *IEEE Journal of Solid-State Circuits*, Vol. 32, No. 12, pp. 1858-1865, December 1997.

[13] H. K. Gummel, H. C. Poon, "An integral charge control model of bipolar transistors", *Bell Systems Technical Journal*, Vol. 49, pp. 827-852, May 1970

[14] Q. Zhang, A. Agarwal, C. Capell, L. Cheng, M. O'Loughlin, A. Burk, and J. Palmour, "SiC Super GTO Thyristor Technology Development: Present Status and Future Perspective," *IEEE*, 2011.

[15] S. C. Glidden and H. D. Sanders, "Solid State Spark Gap Replacement Switches," *IEEE*, 2006.

[16] R. Polij, J. Kennedy, T. Blackwell, "Particle Swarm Optimization: An Overview," *Swarm Intel.*, pp. 33-57, 2007.

[17] A. Fierro, "Particle Swarm Optimization," Personal interview by M. B. Walls, April 2014.

[18] WIMA, "WIMA Snubber FKP Datasheet," wima.com., November 2014.

[19] MK Magnetics, "Nanocrystalline A Special Product Announcement," http://www.mkmagnetics.com/dataSheets/pdf/mkm-brochure-2012-1207.pdf., 2008.

[20] L. Collier, "Magnetic Core B-H Characterization," Personal interview by M. B. Walls, March 2015.

APPENDIX A

SOLUTION TO R-L-C CIRCUIT

A series R-L-C circuit is shown in Fig. A.1.

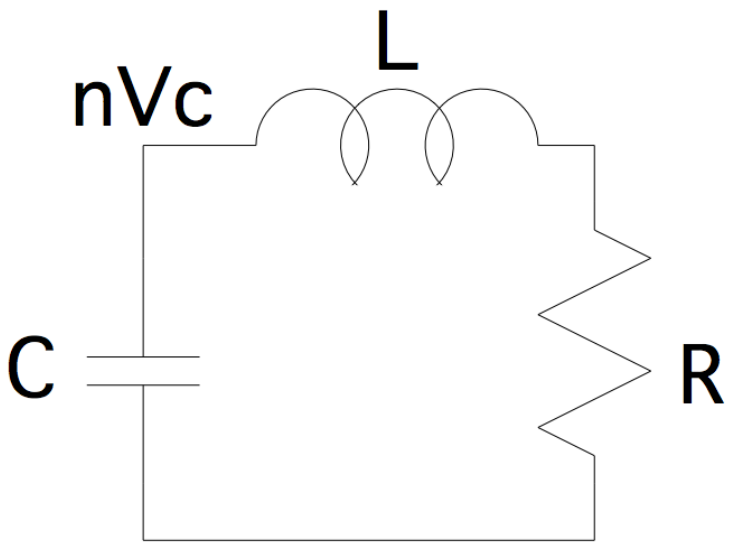

Figure A.1: Example R-L-C circuit. Positive current flows clockwise. Initial current is 0 A. Initial voltage at node nVc is V_0.

In the Laplace domain, Kirchoff's voltage law is expressed in Eq. A.1.

$$-\left(\frac{1}{sC}(-I(s)) + \frac{V_0}{s}\right) + sLI(s) + RI(s) = 0 \tag{A.1}$$

Solving for $I(s)$ gives Eq. A.2.

$$I(s) = \frac{V_0}{s^2L + sR + 1/C} = \frac{V_0}{L\sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}} \frac{\sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}}{\left(s + \frac{R}{2L}\right)^2 + \left(\frac{1}{LC} - \frac{R^2}{4L^2}\right)} \tag{A.2}$$

The known Laplace transform given in Eq. A.3 is used to take the inverse Laplace transform of Eq. A.2, which gives the current as a function of time, given in Eq. A.4.

$$\mathcal{L}\left\{e^{\alpha t}\sin\left(bt\right)\right\}\left(s\right) = \frac{b}{\left(s-\alpha\right)^2 + b^2} \tag{A.3}$$

$$i(t) = \frac{V_0}{\sqrt{\frac{L}{C} - \frac{R^2}{4}}} e^{\left(-\frac{Rt}{2L}\right)} \sin\left(\left(\sqrt{\frac{1}{LC} - \frac{R^2}{4L^2}}\right) t\right) \tag{A.4}$$

This solution is only valid for underdamped cases, where $R < \sqrt{4L/C}$. It is observed from Eq. A.4 that the oscillation is damped by a decaying exponential function with a decay constant given in Eq. A.10.

$$\alpha = \frac{R}{2L} \tag{A.5}$$

Rearranging, the series resistance R can be given in terms of the series inductance L and the decay coefficient α.

$$R = 2\alpha L \tag{A.6}$$

The resonant frequency is seen in the sine function of Eq. A.4, and is given in Eq. A.7. Additionally, an approximation is given for low values of R.

$$f_r = \sqrt{\frac{1}{4\pi^2 LC} - \frac{R^2}{16\pi^2 L^2}} \approx \frac{1}{2\pi\sqrt{LC}} \tag{A.7}$$

Rearranging, the series inductance L can be approximated in terms of the capacitance C and the resonant frequency f_r.

$$L = \frac{1}{4\pi^2 f_r^2 C} \tag{A.8}$$

Fig. A.2 shows an example decaying sinusoidal waveform, with the first two local maxima highlighted.

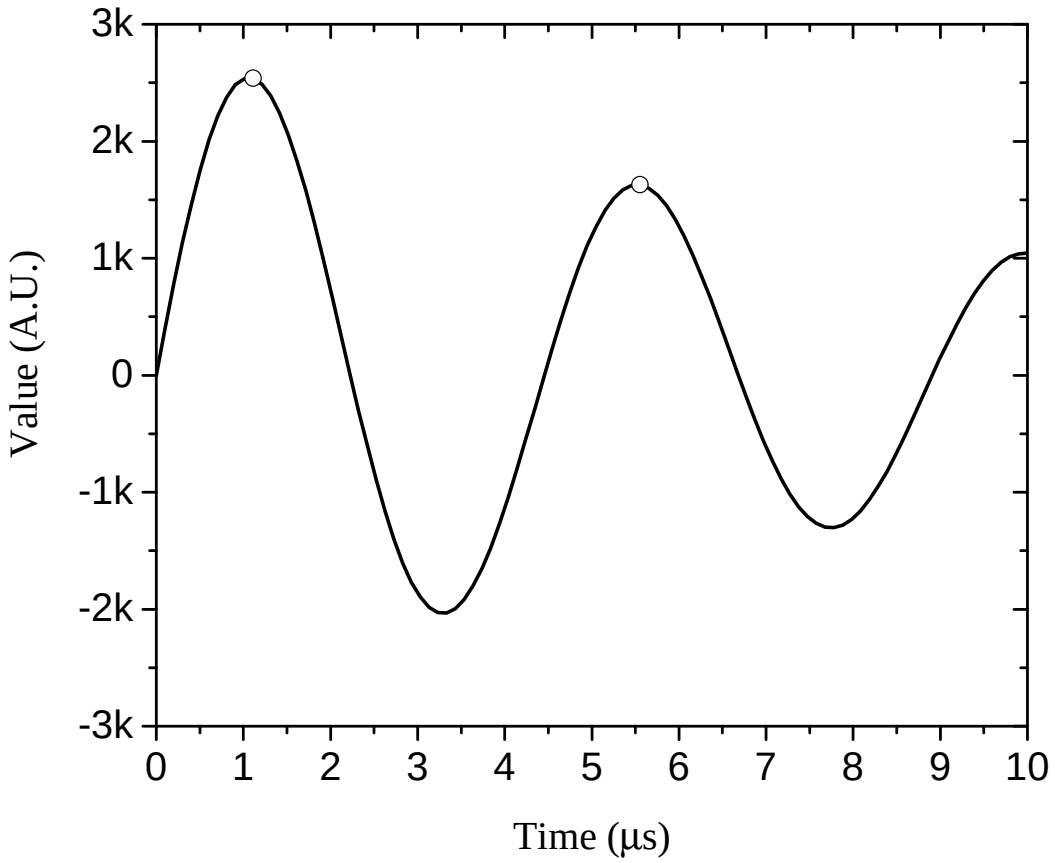

Figure A.2: Example decaying sinusoidal waveform. The first two local maxima are marked.

By observation of any two local maxima, $I_{max,1}$ and $I_{max,2}$, and the times at which the maxima occur, t_1, and t_2, the decay constant α can be calculated using the expression given in Eq. A.12. This is accomplished by first observing the basic form of a exponentially decaying sinusoidal function, as given in Eq. A.9.

$$I(t) = Ae^{-\alpha t}\sin(bt) \tag{A.9}$$

Observation of $I_{max,1}$ and $I_{max,2}$ give two points from the curve described by Eq. A.9. Because these points occur at local maxima in the sinusoidal oscillation, it is assumed at $\sin(bt_1) \approx 1$ and $\sin(bt_2) \approx 1$. Thus, substituting $I_{max,1}$, $I_{max,2}$, t_1, and t_2 gives Eq. A.10.

$$\begin{aligned} I_{max,1} &= Ae^{-\alpha t_1} \\ I_{max,2} &= Ae^{-\alpha t_2} \end{aligned} \tag{A.10}$$

Setting the first equation as the numerator and the second equation as the denominator in a ratio equation, Eq. A.10 can be equivalently expressed in Eq. A.11.

$$\frac{I_{max,1}}{I_{max,2}} = \frac{Ae^{-\alpha t_1}}{Ae^{-\alpha t_2}} = e^{-\alpha t_1 - (-\alpha t_2)} = e^{\alpha(t_2 - t_1)} \tag{A.11}$$

Taking the natural logarithm of both sides of Eq. A.11, and dividing by $t_2 - t_1$, the decay constant is given in Eq. A.12.

$$\alpha = \frac{\ln(I_{max,1}/I_{max,2})}{t_2 - t_1} \tag{A.12}$$

APPENDIX B

CONTINUOUS AND DISCRETE TRANSFORMS AND OPERATIONS

B.1 The Laplace Transform

The Laplace transform is defined by Eq. B.1.

$$\mathcal{L}\left\{f(t)\right\}(s) = F(s) = \int_0^\infty e^{-st} f(t) dt \tag{B.1}$$

The Laplace transform is a special case of the integral transform were the kernel function is e^{-st}. The Laplace transform is used extensively in circuit analysis where the impedance of lumped element inductors is given in the Laplace domain as sL, and the impedance of capacitors is given as $1/sC$.

B.1.1 The Inverse Laplace Transform

The inverse Laplace transform is defined by Eq. B.2.

$$\mathcal{L}^{-1}\left\{F(s)\right\}(t) = f(t) = \frac{1}{2\pi j} \int_{\gamma - j\infty}^{\gamma + j\infty} e^{st} F(s) ds \tag{B.2}$$

The inverse Laplace transform maps a function from the Laplace domain to the time domain. Here, γ is a constant that is set to any arbitrary value that is greater than the real part of all singularities of $F(s)$. For example, if a function $G(s)$ has poles at $s_p = 4 \pm j3$, then γ can be given any value greater than $\Re\{s_p\} = 4$.

In practice, functions of s are mapped to the time domain by algebraically manipulating the function into a certain form that conforms to a known Laplace transform.

For example, Eq. A.3 is a known Laplace transform that is used to take the inverse Laplace transform of Eq. A.2, which yields Eq. A.4. Known Laplace transforms are tabulated.

B.2 The Fourier Transform

The Fourier transform is defined by Eq. B.3.

$$\mathcal{F}\{x(t)\}(\omega) = X(\omega) = \int_{-\infty}^{\infty} e^{-j\omega t} x(t) dt \tag{B.3}$$

Here, ω is the angular frequency in rad/s. ω can be converted to f, given in Hz, by the relation $\omega = 2\pi f$.

Similar to the Laplace transform, the Fourier transform is a special case of the integral transform where the kernel function is the complex exponential $e^{-j\omega t}$. Because Euler's relation, given in Eq. B.4, shows that complex exponentials can be expressed as a real and imaginary sinusoid, the Fourier transform is used to map a time-domain signal to the frequency domain so that the spectral amplitude and/or phase can be analyzed.

$$e^{-j\omega t} = \cos(\omega t) - j\sin(\omega t) \tag{B.4}$$

For analyzing the spectral amplitude of a signal, the magnitude of the Fourier transformed signal can be calculated according to Eq. B.5.

$$|X(\omega)| = \sqrt{\Re\{X(\omega)\}^2 + \Im\{X(\omega)\}^2} \tag{B.5}$$

For analyzing the spectral phase of a signal, the phase angle of the Fourier transformed signal can be calculated according to Eq. B.6.

$$\theta = \sin^{-1} \frac{\Im\{X(\omega)\}}{\Re\{X(\omega)\}} \tag{B.6}$$

B.2.1 The Inverse Fourier Transform

The inverse Fourier transform maps a function from the frequency domain to the time domain, and is defined by Eq. B.7.

$$\mathcal{F}^{-1}\{X(\omega)\}(t) = x(t) = \int_{-\infty}^{\infty} e^{j\omega t} X(\omega) ds \tag{B.7}$$

B.2.2 The Discrete Fourier Transform

The Fourier transform may be discretized and applied to digital signals. The discrete Fourier transform is defined by Eq. B.8.

$$\mathcal{F}_d\{x\}_k = X_k = \sum_{n=0}^{N-1} x_n e^{-j2\pi kn/N} \tag{B.8}$$

Here, x_n represents the $(n+1)^{th}$ value in a set of values that are sampled at a frequency f_s. N is the number of data points in the time-domain signal. The discrete fourier transform yields a vector of N complex numbers that correspond to the k^{th} frequency in a corresponding vector of N frequency values defined by Eq. B.9.

$$f_k = \frac{k f_s}{N-1} \tag{B.9}$$

B.3 Differentiation

Differentiation is the most basic calculus operation. The derivative of a function is defined by Eq. B.10.

$$\frac{df}{dt} = \lim_{\Delta t \to \infty} \frac{f(t + \Delta t) - f(t)}{\Delta t} \tag{B.10}$$

The derivative of a function $f(t)$ with respect to the independent variable t gives the rate of change of f with respect to t.

B.3.1 Discrete Differentiation

Differentiation may be applied to a digital signal by several approximation methods. The most accurate of these is central-difference approximation, and is defined by Eq. B.11.

$$\frac{df}{dt}\left(t = t_n + \frac{\Delta t}{2}\right) = \frac{f_{n+1} - f_n}{\Delta t} \tag{B.11}$$

Here, the derivative is approximated at the halfway point between the t_n and t_{n+1}. f_n and f_{n+1} represent the n^{th} and $(n+1)^{th}$ data point, respectively, and Δt represents the elapsed time between the measurement of the two data points.

B.4 Integration

Integration, or anti-differentiation, is the second fundamental calculus operation, and is defined by Eq. B.12.

$$\int_{t_1}^{t_2} f(t)dt = \lim_{N \to \infty} \sum_{n=0}^{N-1} \left\{ f\left(t_1 + n\frac{t_2 - t_1}{N}\right)\left(\frac{t_2 - t_1}{N}\right)\right\} \tag{B.12}$$

Here, $(t_2 - t_1)/N$ represents an independent variable step, Δt. The result of the summation gives the approximate area under the curve f between the limits t_1 and t_2. As the N approaches infinity, the independent variable step Δt approaches zero, and the resulting summation approaches the exact area underneath the curve f between the limits t_1 and t_2.

B.4.1 Discrete Integration

Integration can be carried out on a digital signal. Several methods are available for integral approximation. The information in this thesis is presented using the trapezoidal integration approximation. Discrete trapezoidal integration is defined by Eq B.13.

$$\int_{t_1}^{t_2} f(t)dt \approx \sum_{n=0}^{N-1} \frac{1}{2}(f(t + n\Delta t) + f(t + (n+1)\Delta t))\Delta t \tag{B.13}$$

Here, Δt represents the sampling period, and n is an integer index referring to the $(n+1)^{th}$ data point. Trapezoidal integral approximation overestimates the integral for signals that are convex with respect to the independent variable, and underestimates the integral for signals that are concave with respect to the independent variable. For very small step sizes, however, this effect becomes negligible.

APPENDIX C

TRANSFORMER THEORY

A transformer is an electrical device that uses coupled inductors to transfer electrical energy from one circuit to another without the need for a physically conductive link between the two circuits. The circuit symbol for a transformer is shown in Fig. C.1, with voltage and current conventions indicated.

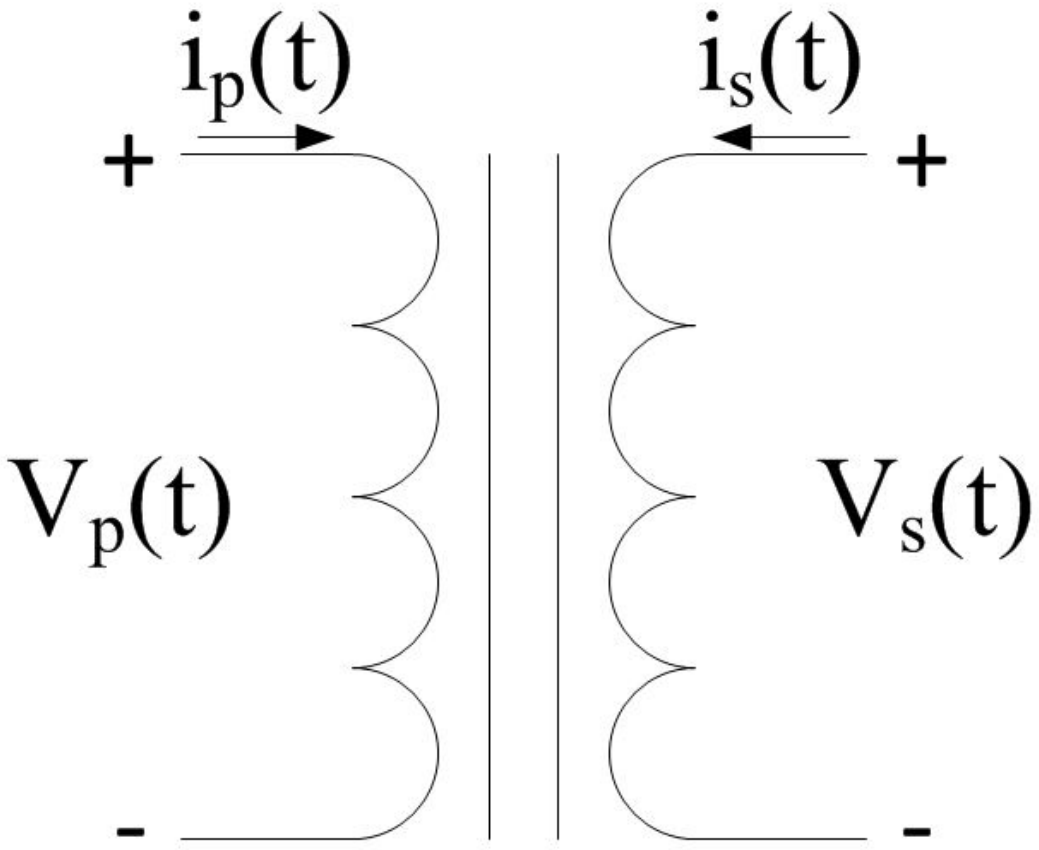

Figure C.1: Transformer circuit symbol. Positive current and voltage polarities are indicated.

A transformer is defined as two inductors with self inductances L_p and L_s, and a mutual inductance M between them. The current-voltage relationship between the primary and secondary terminals is then defined by Eq. C.1.

$$\begin{aligned} v_p(t) &= L_p \frac{di_p}{dt} + M \frac{di_s}{dt} \\ v_s(t) &= L_s \frac{di_s}{dt} + M \frac{di_p}{dt} \end{aligned} \tag{C.1}$$

Assuming perfect coupling, the mutual inductance between primary and secondary inductor is $M = \sqrt{L_p L_s}$. For imperfectly coupled inductors, a coupling coefficient k is defined by Eq. C.2 that characterizes the coupling between the inductors.

$$k = \frac{M}{\sqrt{L_p L_s}} \tag{C.2}$$

An ideal transformer is achieved for $k = 1$, $L_p \to \infty$, and $L_s \to \infty$. Under these conditions, the current and voltage relationship between the primary and secondary terminals resolves to Eq. C.3.

$$\frac{v_s(t)}{v_p(t)} = \sqrt{\frac{L_s}{L_p}} = \frac{i_p(t)}{i_s(t)} \tag{C.3}$$

To achieve a high mutual inductance, real transformers possess a saturable magnetic core with a relative permeability $\mu_r > 1$. Saturable cores are characterized by a B-H curve, which relates the H-field in the material to the B-field, such as the curve shown in Fig. C.2.

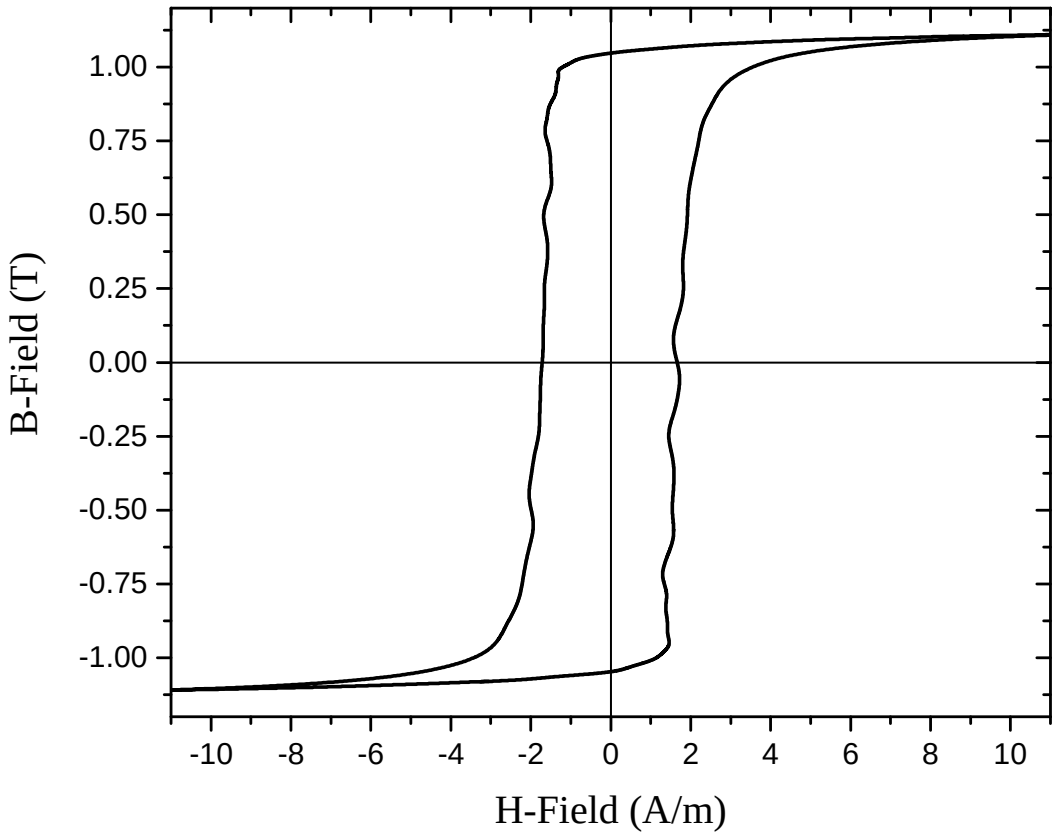

Figure C.2: Example BH curve measured for MK Magnetics Nanocrystalline core material [19, 20].

When the H-field reaches a certain value, the core saturates, and the relative permeability of the material drops to $\mu_r = 1$. For transformers that use such magnetic materials to achieve near ideal coupling, core saturation drastically reduces the coupling coefficient, and thus the performance of the transformer.

Because the transformer core saturates at a particular H-field strength, and the H-field strength is directly proportional to the magnetizing current $i_m(t)$, the transformer can be thought of as saturating at a threshold magnetizing current.

Assuming the transformer is actively driven from the primary terminal only, and the initial magnetizing current is zero, the magnetizing current can be expressed by Eq. C.4.

$$i_m(t) = \frac{1}{L_p} \int_0^t v_p(\tau) d\tau \tag{C.4}$$

The magnetizing current is not equal to the primary current, since the primary current induces a secondary current which opposes the magnetic field created by the primary current. The primary current is instead the current through the primary that would result from the same voltage waveform being applied to the primary, with the secondary terminal open-circuited. Because the magnetizing current is directly linked to core saturation, but may be difficult to predict in design, the core is usually specified as saturating at a given number of volt-seconds. The magnetizing current and the volt-seconds applied to the primary are seen to be equivalent in Eq. C.4.